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Frequency Shift Keying Demodulation Methods For Wireless Biomedical Implants

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Respectfully submitted.

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ABSTRACT

A high data rate frequency shift keying (FSK) data transfer protocol and two different demodulator circuits have been developed with the data-rate to carrier-frequency ratio of up to 67%. The primary application for these novel FSK modulation/demodulation techniques is in the magnetically powered wireless systems such as biomedical implants and radio frequency identification (RFID) tags with high data rates above 1 Mbps. The demodulator circuits extract the serial data bit stream and a constant-frequency clock from an FSK carrier signal in the 1~20 MHz range, which can power the wireless system as well. In the FSK modulation protocol, used in the present invention, a first frequency is assigned for transferring logic value "1" and a second frequency is assigned for transferring logic value "0". However, the second frequency is chosen twice as the first frequency so that the duration of each data bit is the same regardless of its value. The first demodulator circuit, called referenced differential FSK (RDFSK), uses both analog and digital (mixed-signal) techniques to discriminate between the fist and second frequencies in the received FSK carrier signal. The second demodulator circuit is implemented entirely with digital circuitry and called digital-FSK (DFSK) demodulator. Both demodulator circuits are capable of generating a serial data bit-stream and a synchronized constant frequency clock to be used for sampling the serial data bit-stream and storing it in a shift register or memory device. Both demodulator circuits can detect and indicate one sort of error in the received FSK carrier signal based on the said FSK modulation protocol.

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I. FIELD OF THE INVENTION

The present invention relates to modulation and demodulation of frequency shift keyed (FSK) signals and more practically to a mixed-signal FSK demodulator and a digital FSK demodulator with the capability of detecting data rates close to carrier frequencies and generating a synchronized constant frequency clock signal.

II. GENERAL BACKGROUND OF THE INVENTION

The inductive link between two magnetically-coupled coils is now one of the most common methods to wirelessly transfer power and data from the external world to implantable biomedical devices such as pacemakers and cochlear implants [1-3]. However, this is not the only application of data and power transfer via inductive coupling. Radio-frequency identification (RFID), remote sensing, and MEMS are among a few other fields that can highly benefit from this method [4]. Achieving high power transfer efficiency, high data transfer bandwidth, and coupling insensitivity are some of the challenges that one would face in the design of such systems.

Some of the biomedical implants, particularly those which interface with the central nervous system, such as cochlear and visual prostheses, need large amounts of data to simultaneously interface with a large number of neurons through multiple channels. In a simplified visual implant for example, a minimum reasonable resolution of only 32×32 pixels for an image requires 10-bits for addressing, 8-bits for 256 gray levels implemented as pulse amplitude or pulse width, and 2-bits for polarity and parity-checking, which suggests a 20-bit data-packet for each pulse. If we consider the human-eye natural bandwidth of 60 frames/sec, then 1.23 Mbps needs to be transferred to this implant just as pure data. Therefore, a high data-rate receiver circuitry that can establish an efficient wireless link between the implant and the external units is highly needed.

In broadband wireless communications such as IEEE 802.11a standard for wireless LAN application, baud-rates as high as 54 Mbps have been achieved at the expense of increasing the carrier frequency up to 5.8 GHz, giving a data-rate to carrier-frequency ratio of only 0.93%. In other words, each data bit is carried by 107.4 carrier cycles. However, the maximum carrier frequency for biomedical implants is limited to a few tens of MHz due to the coupled coils self-resonant frequency, more power loss in the power transfer circuitry at higher frequency, and excessive power dissipation in the tissue, which increases as square of the carrier frequency [5]. Therefore, the goal of this invention is to transfer each data bit with a minimum number of carrier cycles to maximize the data-rate to carrier-frequency ratio and minimize the amount of power consumption.

So far, amplitude shift keying (ASK) data modulation has been commonly used in biomedical implants because of its fairly simple modulation and demodulation circuitry [1, 3, 4, 6-8]. ASK, however, faces major limitations for high-bandwidth data transfer, because high-bandwidth ASK needs high order filters with sharp cut-off frequencies, whose large capacitors cannot be easily integrated in this low-frequency range of RF applications. A remedy that is proposed in the so called suspended carrier modulation [1, 3, 4] boosts the modulation index up to 100% to achieve high data rates with low-order integrated filters at the expense of an average 50% reduction in the transferred power. Therefore, based on the facts provided in the following,

we believe that the FSK data modulation is a superior technique for wirelessly operating those applications such as biomedical implants and RFID tags, in need of high data rates in excess of 1Mbps, while utilizing low frequency carrier signals. A sample implementation of this invention has been used for wirelessly operating the University of Michigan micromachined stimulating 3D-microprobes, shown in Fig. 1, which are targeted at a 1024-site wireless stimulating microsystem for visual and auditory prostheses [7-9].

III. FSK DATA TRANSFER PROTOCOL INVENTION

A. FSK Data Transfer Protocol Background

In simple terms, a digital data signal may be used to modulate the amplitude, the frequency, or the phase of a carrier signal depending on the particular application. These three types of modulation are known as amplitude shift keying (ASK), frequency shift keying (FSK), and phase shift keying (PSK) respectively. In any of these modulation techniques, the modulated carrier signal takes on one of two states, i.e. one of two amplitudes, two frequencies, or two phases to represent either logic "0" or logic "1".

FSK is one of the most common modulation techniques for digital communication, which as denoted above, simply means sending binary data with two frequencies f_0 and f_1, representing logic "0" and logic "1" respectively. The resultant modulated signal can be regarded as the sum of two complementary 100% amplitude-modulated signals at different carrier frequencies as shown in Fig. 2a.

$$f(t) = f_0(t)\sin(2\pi f_0 t + \phi) + f_1(t)\sin(2\pi f_1 t + \phi) \tag{1}$$

The reciprocals of these two frequencies, i.e. $1/f_0$ and $1/f_1$, are denoted by T_0 and T_1 respectively throughout this document and they are the information carrying entities in FSK modulation as well as parameters of interest to indicate the type of received signal in the present invention.

In the frequency domain, the signal power is centered at two carrier frequencies, f_0 and f_1, as shown in Fig. 2b. Since $f_0(t)$ and $f_1(t)$ can have the same amplitude, an excellent characteristic of the FSK modulation for those wireless biomedical implants and RFID applications, which do not include any internal power source such as a battery and should be electromagnetically powered through the inductive link, is that the transmitted power is always constant at its maximum level irrespective of f_0 and f_1 or the data content.

$$|f_0(t)| = |f_1(t)| = V_m \Rightarrow V_{rms}(f) = {}^{1}\!/\!_{\sqrt{2}}\, V_m \tag{2}$$

Another difference between the FSK and ASK is that in ASK data transmission the receiver tank circuit frequency response should have a very high quality factor (Q), centered at the carrier frequency to get enough amplitude variation for data detection. However, in our FSK data transmission, the pass band should be centered between f_0 and f_1 with a low Q to pass enough power of both carrier frequencies. This is an advantage for the FSK technique because in the biomedical implant applications, the quality factor of the tiny receiver coil is inherently low particularly when the implant receiver coil is integrated and its high resistivity is unavoidable [6]. In addition, the FSK signal is much less susceptible to the coupled coils misalignment and

motion artifacts which are two major problems seen in biomedical implants that adversely affect the amplitude of the received signal.

Synchronization of the receiver with the transmitter is however easier in the ASK and PSK systems compared to FSK. Because the receiver internal clock signal that is usually used to sample the detected serial data bit stream can be directly derived by stepping down the constant transmitter carrier frequency, which can also be synchronized with the carrier data contents by the external transmitter [6-8]. In FSK modulation, on the other hand, there is no constant frequency and the recovered data bit stream should be sampled either by asynchronous means in which the data phase jitter can cause erroneous readings at high data rates or by an internal clock with constant frequency which should be derived from a combination of the two carrier frequencies (f_0 and f_1) based on the data transfer protocol, as is done in the present invention, or synchronization patterns.

B. Preferred Embodiment of the FSK Data Transfer Protocol

A principal objective of the present invention is to maximize the data-rate to carrier-frequency ratio. Therefore, a particular protocol was devised for the FSK data transfer with data-rate as high as f_1 with f_0 twice as f_1 where f_0 and f_1 are the first and second frequencies chosen for representing logic "0" and logic '1" respectively. In the preferred protocol presented in this invention, the logic bit "1" is transmitted by a single cycle of the carrier f_1 and the logic bit "0" is transmitted by two cycles of the carrier f_0 as shown in Fig. 2a. The transmitter frequency switches at a small fraction of a cycle and only at negative-going zero crossings, which means at the end of a full carrier cycle. This leads to a consistent data transfer rate of f_1 bits per second. As a result, if we consider the average carrier frequency to be $(f_0+f_1)/2$, then the data-rate to carrier-frequency ratio can be as high as 67%.

It is another objective of the present invention to derive a constant frequency clock signal from a combination of the two carrier frequencies (f_0 and f_1) to be used for sampling the demodulated serial data bit stream at a constant rate as well as any other timing purposes.

It is also useful to notice that any odd number of consecutive f_0 cycles in this protocol is an indication of data transfer error. Therefore it is yet another objective of this invention to indicate these kinds of errors and remove them from the recovered serial data bit stream.

IV. FSK DEMODULATION

A. FSK Demodulator Background

All of the conventional FSK demodulation techniques such as FM discriminator, phase locked loop (PLL), or quadrature detector need some kind of analog filtering down the signal path, which need off-chip resistive or capacitive components or consume a large chip area if implemented on-chip due to the low range radio frequency (RF) applications of the present invention. Therefore, in the present invention we have tried to deal with the received FSK carrier as a base-band signal and eliminate any types of mixing or filtering, thus eliminating most of the problems associated with fully analog FSK demodulation techniques learnt from the prior art. The data detection technique used in the present invention for FSK demodulation is based on measuring the period of each received carrier cycle, which is the information carrying entity in FSK modulation scheme, by analog or digital means and then decide on the received data-bit

value based on that parameter. If the measured period is higher than a certain threshold value (either analog or digital), a logic "1" bit is detected and otherwise a logic "0" is received.

B. Preferred Embodiments of the Mixed-Signal FSK demodulator Circuit

A simple method for time measurement in an analog circuit is charging a capacitor with a constant current source and monitoring its voltage due to the linear relationship between the capacitor voltage and time in this situation. Therefore, according to one embodiment of the present invention, duration of every carrier cycle can be measured by charging a capacitor in half of a cycle and discharging it in a short fraction of the other half. It should be noted that charging and discharging of this capacitor should be synchronized with the FSK carrier signal. If the capacitor voltage goes higher than a certain threshold value, a logic "1" bit is detected and otherwise a logic "0" is received.

According to the first embodiment of the present invention called referenced differential FSK demodulator (RDFSK): A single capacitor is charged with a single current source during the first (negative) lobe of the sinusoidal FSK carrier signal and its voltage has been compared with a constant reference voltage using a hysteresis comparator as shown in Fig. 3. The output of the hysteresis comparator asserts after a long half cycle ($T_1/2$) but not after a short half cycle ($T_0/2$) because the width of the hysteresis window, W_{hyst}, has been adjusted somewhere between the capacitor and reference voltage difference at the end of the first half cycles (V_0-$V_{ref} < W_{hyst} < V_1$-V_{ref}). This is how the RDFSK circuit is capable of discriminating between the long and short FSK carrier cycles. The capacitor is then discharged in a fraction of the second (positive) lobe of the FSK carrier signal to be ready for detection of the type of the next cycle. An implementation of a prototype demodulator chip based on the RDFSK method, fabricated at the AMI 1.5-μm 2-metal 2-poly standard CMOS process through the commercial MOSIS foundry, is shown in Fig. 4 [10], [11].

Fig. 5 shows the RDFSK demodulator block diagram. The FSK carrier signal in its sinusoidal form is picked up directly across the receiver tank circuit, which usually consists of a parallel or series combination of one or more capacitors and a receiver coil. The oscillation frequency of the tank circuit should be adjusted around the average of the carrier frequencies, $(f_0 + f_1)/2$, in order to receive both frequencies with the same amplitude. However, the demodulator performance is not sensitive to this frequency and possible amplitude modulation of the carrier signal due to the proximity of the oscillation frequency of the tank circuit to one of the FSK carrier frequencies. The quality factor (Q) of the tank circuit in the present invention should be low enough to pass most of the FSK carrier energy that is centered on f_0 and f_1 as shown in Fig. 2b. This is usually the case in small implantable coils in biomedical implants or planar coils in RFID tags due to their inherent parasitic resistance; however, it can also be further adjusted by adding a resistor to the LC-tank circuit.

The clock recovery circuit (also called clock regenerator) is a high gain comparator with hysteresis, which is directly connected to the receiver tank circuit as shown in Fig. 5. This block squares up the sinusoidal FSK carrier waveform and converts it into a similar square digital waveform called CK_{in}. The clock recovery block is a cross-coupled differential pair as shown in Fig. 6. The positive feedback, which is implemented by the cross-couple load in this circuit, gives it a very large gain, which is required to provide sharp edges for the CK_{in} signal. The hysteresis effect which is provided by the threshold voltages of the input pMOS differential pair

avoids this circuit from reacting to noise or any low amplitude artifact added to the sinusoidal FSK carrier due to the coil mechanical vibrations for example. The output of the cross-coupled differential pair is buffered before being applied to the data detector and digital blocks.

Fig. 7 shows a simplified schematic diagram of the RDFSK data detector circuit. Both S_1 and S_2 switches are controlled by CK_{in}. When CK_{in} is low, S_1 switch is closed and S_2 is open. Therefore, I_C current source linearly charges the capacitor C. During a logic "1" long cycle, C is charged up to V_1, which is twice as V_0 when a logic "0" short cycle is being received. A hysteresis comparator compares the capacitor voltage with a constant 1.26V bandgap voltage reference, V_{ref}, which is shown as a constant DC voltage source in Fig. 7. The bandgap voltage reference is well known among those skilled in the art and has a good stability over temperature and process variations. The hysteresis window width of the hysteresis comparator, W_{hyst}, is set somewhere between V_1-V_{ref} and V_0-V_{ref}. Therefore, the comparator output switches to high during a logic "1" long cycle but not during a logic "0" short cycle. The S_2 switch discharges the capacitor in a fraction of the FSK carrier 2nd half cycle, when CK_{in} is high. Meanwhile, the S_1 switch is open to shut down I_C current and reduce power consumption. CK_{in} also resets the hysteresis comparator to its initial status to prepare it for detecting the type of the next cycle. The FSK square pulses which are generated by the hysteresis comparator only at the end of long carrier half cycles discriminate them from the carrier short half cycles.

The output of the RDFSK data detector circuit, called FSK, is only a series of pulses, which discriminate between long and short FSK carrier cycles. So it cannot be directly regarded as the received data bit stream. These pulses are fed into a digital block along with CK_{in} to generate the serial data bit stream output (*Data-Out*) and a constant frequency clock (*Clock-Out*). Fig. 8 shows the schematic diagram of the digital block. On every rising edge of CK_{in} at the end of the 1st half of an FSK carrier cycle, a 2-bit shift register (flop-flops 1 and 2) shifts in the FSK signal logic values from data detector block. According to the FSK protocol of the present invention, every 2 successive short cycles should produce a logic "0" bit on the *Data-Out* output and every single long cycle should produce a logic "1" bit. Therefore, *Data-Out* is generated by connecting the shift register output terminals to an OR (NOR + Inverting buffer) gate.

To generate a constant frequency clock, a T flip-flop (flip-flop 3) indicates the number of successive short cycles such that its output is high when the number of received successive short cycles is odd. Another T flip-flop (flip-flop 4) toggles on every long CK_{in} cycle or two successive short CK_{in} cycles. The resulting signal at the output of flip-flop 4 is a clock signal with constant frequency equal to $f_1/2$ irrespective of the data contents. In order to achieve the highest data rate, *Data-Out* serial bit stream should be sampled at both rising and falling edges of this output clock signal (*Clock-Out*). Therefore, *Clock-Out* is delayed by two 4-input NAND gates and two inverting buffers to provide the serial data bit stream output (*Data-Out*) with enough time to stabilize before any rising or falling edges of the *Clock-Out* sampling signal.

According to the preferred FSK modulation protocol of the present invention, any odd number of short cycles in the received FSK carrier signal is an indication of error and activates the error flag (Error_). To generate the error signal, the output of flop-flop 3 which counts the number of successive short cycles and the incoming FSK signal from data detector block are applied to a NAND gate. If both of these inputs become high at the same time, it means that there is an incoming long carrier cycle after an odd number of previous short carrier cycles which is not right and as a result the error flag (Error_) goes low. Another effect of this situation

is that the error flag prevents flip-flop 4 from generating a new sampling edge on the Clock-Out signal thus ignoring the last short cycle in the data bit stream which has produced this error.

To check the performance of the RDFSK demodulator, post-layout simulation was performed by choosing f_1 and f_0 to be 4MHz and 8MHz respectively as shown in Fig 9. The data bit stream of "0000111100110011" {1} is modulating the FSK carrier {2}, which is fed into the RDFSK demodulator circuit. The clock recovery block converts the sinusoidal input to a square waveform, CK_{in}, which is shown on trace {3}. The capacitor and reference voltages {4} are the inputs to the hysteresis comparator, which indicates long carrier cycles by generating the FSK pulses {5}. The FSK pulses {5} and CK_{in} {3} are the inputs to the digital block, which in turn generates the output data bit-stream {6} and a synchronous constant frequency clock {7}. It should be noted that since the output clock rate is $f_1/2$, the data values should be read at both rising and falling edges of the *Clock-Out* signal {7}.

C. Preferred Embodiment of the Digital FSK Demodulator Circuit

Analog blocks usually occupy more area than their digital counterparts and are more susceptible to process and temperature variations. Their design also becomes more challenging with the trend towards smaller feature size and lower power supply voltage. Therefore, a fully digital demodulator can save a lot of chip area, make a mixed-signal design more homogeneous, and ease many of the above problems.

In the digital approach to the objectives of the present invention, we measure the duration of every FSK carrier positive half cycle by a timer/counter that runs with a constant-frequency clock time-base (f_{TB}) at a rate several times higher than the FSK carrier frequencies, which is generated by a local oscillator. In many cases this local oscillator, which does not need to be synchronized with the carrier, is already available in the system for running other digital circuits or a microprocessor. In this embodiment of the present invention, an n-bit counter runs by the local oscillator only during the positive lobe of an FSK carrier cycle and measures half of the carrier cycle duration. During the negative lobe of the FSK carrier, the counter stops and a digital comparator decides whether a long or short carrier cycle has been received by comparing the counter value with a constant reference number. Then it resets the counter for measuring the duration of the next cycle [12].

The time-base period ($1/f_{TB}$) should be smaller than the time-difference between $T_0/2$ and $T_1/2$ half-cycles for the digital FSK demodulator (D-FSK) to be able to discriminate between these two frequencies. In other words f_{TB} should be chosen based on:

$$f_{TB} > \frac{2 f_1 f_0}{f_0 - f_1} \tag{3}$$

and the minimum width of the counter (n) should satisfy:

$$2^n > f_{TB}/2f_1 \quad \text{or} \quad n > \log_2(f_{TB}/2f_1) - 1 \tag{4}$$

In order to make the demodulator circuit simpler and reduce dynamic power consumption, the digital comparator can be combined with the counter by choosing f_0, f_1, f_{TB} and n so that:

$$f_{TB}/f_1 > 2^n > f_{TB}/f_0 \tag{5}$$

In this case, the most significant bit (MSB) of the counter determines whether a long or short FSK carrier cycle has been received and the constant reference number is equal to 2^n. This algorithm was implemented in a prototype chip, which is shown in Fig. 10 and fabricated in the AMI 1.5-μm 2-metal 2-poly standard CMOS process through the commercial MOSIS foundry.

The block diagram of Fig. 11 shows the entirely digital embodiment of the present invention. The sinusoidal FSK carrier signal is directly picked across the receiver tank circuit and squared up by the clock recovery block to provide the input clock signal (CK_{in}) to the D-FSK circuit. An n-bit counter runs by a local ring oscillator which generates a time-base clock (TB) at f_{TB} which is several times higher than the FSK carrier frequencies. The counter MSB ($C2$) indicates the FSK carrier long cycles and enters a digital block along with CK_{in}. The digital block, which is the same as the one used in FDFSK and RDFSK embodiments and shown in Fig. 8, converts C2 pulses to the output serial data bit stream (Data-Out). It also generates a constant frequency output clock (Clock-Out) for sampling individual data bits as well as an error flag (Error_) indicating any odd number of short FSK carrier pulses.

According to the FSK data-transfer protocol of the present invention, exemplary values were chosen for f_0 and f_1 equal to 8MHz and 4MHz respectively to achieve data-rates as high as 4Mbps. By choosing these frequencies for the FSK carrier in this example, equation (3) sets a lower limit for the time-base clock ($f_{TB} > 16$ MHz); and by choosing the counter width $n = 3$, equation (5) defines a new range for f_{TB} (64 MHz $> f_{TB} >$ 32 MHz), which satisfies (3) as well. Therefore, a 5-stage ring-oscillator was designed for the local oscillator to generate $f_{TB} = 49$ MHz at the center of the above range. It should be noted that the scheme presented in this embodiment of the present invention is highly robust and as long as f_{TB} is in the desired range, the phase noise and frequency variations of the local oscillator, up to 30%, do not affect the demodulation process.

Fig. 12 shows the schematic diagram of the D-FSK demodulator and Fig. 13 shows sample simulation waveforms when "001111001100l1" data bit-stream is FSK modulated and applied to the D-FSK demodulator circuit {1}. The clock-regenerator circuit is a cross-coupled differential pair similar to the one used in mixed-signal demodulators and shown in Fig. 7. This block is directly connected to the receiver tank circuit and turns the sinusoidal FSK carrier signal {2} into a similar square digital waveform called CK_{in} {3}. The internal ring-oscillator generates a time-base clock at f_{TB}, which runs the 3-bit counter after being gated by CK_{in} {4}. When CK_{in} is high, the counter is running; however, it freezes when CK_{in} is low because it does not deceive any more clock pulses. The counter MSB (C_2) stays low during short (62.5ns) carrier half-cycles when count < 4, but goes high during a long (125ns) carrier half-cycle when count ≥ 4 {5}. The counter resets after a short delay when CK_{in} goes low during the 2nd carrier half-cycle to be ready for detecting the type of the next cycle. The MSB of the counter (C_2) provides a series of pulses, which discriminate between long and short FSK carrier cycles {5}. However, they cannot be directly regarded as the received data bit stream. These pulses are fed into a digital block along with CK_{in} {3} to generate the serial data output (*Data-Out*) {6} and a constant frequency clock (*Clock-Out*) {7}. This part of the D-FSK demodulator circuit is the same as the digital block in RDFSK demodulator, which was shown in Fig. 8 and described above.

V. MEASUREMENT RESULTS

A. Mixed-Signal FSK Demodulator Chip

The data detector, clock regenerator, and digital blocks of the RDFSK chip, shown in Figure 4, were tested individually as well as together as an FSK data demodulator chip. All of these circuits were functioning as expected from the simulations up to 200Kbps, which was the highest FSK modulation rate of our function generator (Agilent 33250A). Fig. 14 shows some of the measured waveforms from the RDFSK demodulator chip, while f_1 and f_0 are set to 3 MHz and 6 MHz respectively. All of the traces are labeled according to their names in the simulation and circuit diagrams. It can be seen that the FSK demodulator chip is functioning as expected from the simulations at 200Kbps.

B. Digital FSK Demodulator Chip

The ring-oscillator, clock regenerator, and digital demodulator blocks on D-FSK chip, shown in Fig. 13, were tested both individually and together as a digital FSK demodulator chip. With a 5V supply, the ring-oscillator generates f_{TB} at 50.5 MHz, which is very close to the target value of 49 MHz and is inside the desired range (64 MHz > f_{TB} > 32 MHz). Fig. 19 shows some of the measured waveforms, while f_0 and f_1 are set to 8 MHz and 4 MHz respectively. It can be seen that the FSK demodulator chip is functioning as expected from the simulations at 200 Kbps. A dedicated transmitter is under construction, which will be capable of modulating up to 10Mbps serial data bit-stream out of a fast digital I/O card (NI-6534).

VI. SUMMARY

We have developed a high-rate FSK data transfer protocol and two demodulator circuits for wirelessly operating the University of Michigan micromachined stimulating 3D-microprobes with over 1000 stimulating sites. However, these circuits can be used for any other wireless application, in need of above 1 Mbps data transfer rate through an inductive coupling such as RFID systems. The input clock (CK_{in}) is regenerated from the FSK carrier in 1~20 MHz range, which is used to power the implant as well. The serial data bit-stream (*Data-Out*) and a constant frequency clock (*Clock-Out*) are then extracted from CK_{in}. The RDFSK and D-FSK chips have been designed and fabricated in the AMI 2-metal 2-poly 1.5-μm standard CMOS process, occupying an area of 0.41 mm^2 and 0.29 mm^2 respectively. The prototype chips and their individual blocks are tested at 200Kpbs and were fully functional. Some of the test results and specifications of these two demodulation techniques are summarized and compared in Table 1.

REFERENCES CITED

No.	Patent Number	Date	Cor. [1]	Comments
1	5,684,837	11/1997	1	This patent proposes a very similar FSK modulation protocol and its circuitry is closer to the D-FSK demodulator but it is more complicated and does not recognize errors.
2	4,616,187	10/1986	1	It has very simple logic and it is fully digital similar to D-FSK but it does not generate constant frequency clock for sampling the output data bit stream.
3	3,611,298	10/1971	1	It is digital and uses gated local oscillator to generate high frequency time base similar to D-FSK but it does not generate constant frequency for sampling the output data bit stream.
4	3,623,075	11/1971	1	It has error detection for the situation when there is no good signal. It does not generate constant frequency clock. Input stage is analog.
5	4,021,744	5/1977	2	An analog filter is used for generating serial data output. No constant frequency clock.
6	3,979,685	9/1976	2	Fully digital design. No constant frequency clock. It cannot achieve high data rates.
7	3,846,708	11/1974	2	Very complicated digital circuitry to eliminate data phase jitter which is inherently small in the present invention. No constant frequency clock.
8	3,908,169	9/1975	2	Complicated digital circuitry to add some means for averaging with consecutive counters. No constant frequency clock.
9	5.533.061	7/1996	3	Dedicated to RFID application. Cannot achieve high data rates. No constant frequency clock.
10	4,115,738	9/1978	3	Fully digital. Fairly complex circuitry. Cannot achieve high data rates. No constant frequency clock.
11	3,660,771	5/1972	3	Analog filter used for generation of serial data bit stream. No constant frequency clock.

[1] The degree of correlation to the present invention from high (1) to low (10).

12	5,550,505	8/1996	4	Cannot achieve high data rates. No constant frequency clock.
13	4,551,846	11/1985	4	Fully digital. Suitable for low signal to noise carrier. No constant frequency clock.
14	3,600,680	8/1971	4	The serial data bit stream is generated by analog means. No constant frequency clock.
15	5,399,333	8/1994	5	This is mostly a software implementation. Cannot achieve high data rates. No constant frequency clock.
16	4,488,120	12/1984	6	FSK demodulator using a PLL and voltage comparator
17	5,649,296	7/1997	6	Full duplex modulated back scatter system
18	4,485,347	11/1984	6	Digital FSK demodulator
19	4,368,439	1/1983	6	FSK system
20	4,825,452	4/1989	6	Digital FSK demodulator
21	6,144,253	11/2000	6	Digital FSK demodulator
22	4,103,244	7/1978	6	FSK demodulator
23	4,987,374	1/1991	6	FSK demodulator
24	5,748,036	5/1998	6	Non-coherent digital FSK demodulator
25	5,155,446	10/1992	6	Digital FSK demodulator
26	4,568,882	2/1986	6	Digital FSK demodulator circuit
27	4,752,742	6/1988	6	Frequency demodulator for recovering digital signals
28	4,785,255	11/1988	6	Digital FSK signal demodulator
29	5,245,632	9/1993	6	Synchronous FSK detection
30	4,486,715	12/1984	6	FSK demodulator
31	4,533,874	8/1985	6	Digital FSK demodulator using non-recursive transversal filter
32	4,529,941	7/1985	6	FSK demodulator utilizing multiple-phase reference frequencies

33	6,359,942 B1	3/2002	6	FSK demodulator
34	5,724,001	3/1998	6	Method and apparatus for demodulating FSK signal
35	6,038,268	3/2000	6	Direct conversion FSK signal radio receiver
36	3,636,454	1/1972	7	Digital circuit discriminator for FSK data signals
37	6,501,807 B1	12/2002	7	Data recovery system for RFID interrogator
38	3,539,828	11/1970	7	Frequency discriminator-detector for data transmission system of the FSK type
39	4,010,323	3/1977	7	Digital timing recovery
40	5,953,386	9/1999	7	High speed clock recovery circuit using complimentary dividers
41	4,773,085	9/1988	7	Phase and frequency detector circuits
42	3,512,087	8/1967	7	Frequency modulation receivers for data transmission
43	3,501,704	3/1970	7	FSK demodulator
44	3,947,769	3/1976	7	Threshold correction system in FSK transmissions
45	5,053,717	10/1991	7	FSK demodulator
46	3,614,639	10/1971	7	FSK digital demodulator with majority decision filtering
47	3,949,313	4/1976	7	Demodulation system for digital information
48	4,485,448	11/1984	7	Apparatus and method for detecting the onset of a FSK signal
49	5,436,590	7/1995	7	Digital FSK demodulator with automatic offset cancellation
50	5,394,109	2/1995	7	Digital FSK demodulator with offset cancellation
51	4,716,376	12/1987	7	Adaptive FSK demodulator and threshold detector
52	5,309,113	5/1994	7	FSK data demodulator

53	3,427,614	2/1969	7	Wireless and radioless (nonradiant) telemetry system for monitoring conditions
54	5,583,180	1/1996	8	Data and clock recovery circuit
55	4,363,002	12/1982	8	Clock recovery apparatus for PSK encoded data
56	4,513,427	4/1985	8	Data and clock recovery system for data communication controller
57	6,307,413 B1	10/2001	8	Difference-free clock generator and data recovery PLL
58	5,317,309	5/1994	8	Dual mode electronic identification system
59	6,122,329	9/2000	8	RFID interrogator signal processing system for reading moving transponders
60	3,740,669	6/1973	8	M-ARY FSK digital modulator
61	4,451,792	5/1984	8	Auto-tuned frequency discriminator
62	5,781,064	7/1998	9	Digital filtering system for filtering digital outputs of a four level FSK demodulator
63	5,329,258	7/1994	9	Multilevel FSK modulator having PLL with controlled transient response
64	3,773,975	11/1973	9	FSK digital transmitter
65	3,991,389	11/1976	9	Digital FSK modulator
66	5,621,755	4/1997	9	CMOS technology high speed digital signal transceiver
67	6,366,135 B1	4/2002	9	Data frequency detector
68	5,105,466	4/1992	9	CMOS digital clock and data recovery circuit
69	3,372,234	2/1964	10	Pulse signal demodulator with judgment level producing and comparison means
70	4,543,953	10/1985	10	Analog telemetry system for biomedical implant

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LIST OF FIGURES

LIST OF TABLES

A Wideband Frequency Shift Keying Wireless Link for Inductively Powered Biomedical Implants

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ABSTRACT

A high data-rate frequency shift keying (FSK) modulation protocol, a wideband inductive wireless link, and two demodulator circuits have been developed with a data-rate to carrier-frequency ratio of up to 67%. The primary application of this novel FSK modulation/ demodulation technique is to send data to inductively powered wireless biomedical implants at high data rates above 1Mbps. It can be used in other applications such as RFID tags and contactless smartcards as well. The demodulator circuits detect data bits by directly measuring the duration of each received FSK carrier cycle and also derive a constant frequency clock that is used to sample the data bits. The FSK carrier signal, which is in 1~25MHz range, also powers the wireless device after being rectified. The digital FSK demodulator block occupies 0.29mm^2 in the AMI 1.5-µm 2M/2P standard CMOS process and consumes 0.38mW at 5V. This circuit is simulated up to 4Mbps and experimentally tested up to 2.5Mbps with a bit error rate of 10^{-5}, while receiving a 5/10MHz FSK carrier signal.

INDEX TERMS

Biomedical Implants, CMOS, Data-rate, Demodulator, Inductive Coupling, Frequency Shift Keying, Radio Frequency, RFID, Wireless

I. INTRODUCTION

An inductive link between two magnetically-coupled coils is now one of the most common methods to wirelessly send power and data from the external world to implantable biomedical devices such as neuromuscular stimulators, cochlear implants, and visual prostheses [1]-[8]. However, these are not the only applications of data and power transfer via inductive coupling. Radio-frequency identification (RFID), contactless smartcards, and wireless micro electro-mechanical systems (MEMS) are among a few other fields that can highly benefit from this technique, where the use of batteries is avoided due to extreme size, cost, and lifetime constraints [9]-[12]. Achieving high power transfer efficiency, high data transfer bandwidth, and coupling insensitivity are some of the challenges in the design of such systems. Power transfer efficiency and coupling insensitivity are discussed in [1]-[4]. The main focus of this paper is on the high data transfer bandwidth.

Some of the biomedical implants, particularly those which interface with the central nervous system, such as cochlear and visual prostheses, need large amounts of data to simultaneously interface with a large number of neurons through multiple channels. It is shown that a minimum of 1000 pixels is needed in a visual prosthesis to enable a patient to read text with large fonts [13], [14]. Every stimulation command in such prosthesis requires 10-bits for addressing the stimulating sites, 6 to 8 bits for stimulation pulse amplitude levels, and 2 to 4 bits for polarity, parity-checking, and sequencing. This would suggest at least 20-bits per command-frame for site selection and amplitude information. Considering the human-eye natural bandwidth of 30 frames per second and four commands per biphasic-bipolar stimulation pulse [15], raster scanning all 1000 sites at this rate requires a serial data bit stream of 1000-sites × 20-bits × 4-commands ×

30-frames = 2.4Mbps. Therefore, high data-rate receiver circuitry that can establish an efficient wireless link between the implant and the external units is needed.

In broadband wireless communications such as IEEE-802.11a standard for wireless LAN application, baud-rates as high as 54Mbps are achieved at the expense of increasing the carrier frequency up to 5.8GHz, yielding a data-rate to carrier-frequency ratio of only 0.93%. In other words, each data bit is carried by 107.4 carrier cycles. However, the maximum carrier frequency for biomedical implants is limited to a few tens of MHz due to the coupled coils self-resonant frequency, increased power loss in the power transfer circuitry at higher carrier frequencies, and excessive power dissipation in the tissue, which increases as the carrier frequency squared [16]. Therefore, the goal is to transfer each data bit with a minimum number of carrier cycles to maximize the data-rate to carrier-frequency ratio and minimize power consumption.

So far, amplitude shift keying (ASK) is commonly used in the above applications because of its fairly simple modulation and demodulation circuitry [3]-[12], [17]-[19]. This method however, faces major limitations for high-bandwidth data transfer. Because, high-bandwidth ASK needs high order filters with sharp cut-off frequencies, whose large capacitors cannot be easily integrated in this low-frequency end of RF applications. A remedy that has been proposed in the so called suspended carrier modulation [5], [8], [12] boosts the modulation index up to 100% to achieve high data rates with low-order integrated filters at the expense of an average 50% reduction in the transferred power.

The FSK modulation scheme is utilized in this work to significantly increase the data transfer bandwidth in the previous state-of-the-art designs for wirelessly operating the University of Michigan wireless microstimulating arrays that are targeted at 1024 sites for visual and auditory prostheses [20], [21]. Section II introduces the proposed FSK modulation protocol and compares

it with the typical ASK modulation scheme. Section III describes the demodulation circuitry along with simulation results. Section IV shows a wideband inductive link that is developed to support the proposed FSK modulation/demodulation scheme. Section V covers the experimental measurement results followed by the concluding remarks in section VI.

II. FSK MODULATION PROTOCOL

FSK is one of the common modulation schemes in digital communication, which simply means sending binary data with a sinusoidal carrier at two frequencies, f_1 and f_0, representing logic "1" (mark) and logic "0" (space), respectively. Consequently, in the frequency domain, the signal power is centered about these two frequencies. The FSK signal can be considered as the summation of two complementary ASK signals, $f_0(t)$ and $f_1(t)$, with 100% modulation index. Since $f_0(t)$ and $f_1(t)$ sinusoids usually have the same amplitude, V_m, an excellent characteristic of the FSK modulation for inductively powered wireless devices is that the transmitted power is always constant at its maximum level irrespective of f_0, f_1, frequency modulation index, or the data contents.

$$|f_0(t)| = |f_1(t)| = V_m \Rightarrow P_{rms}(FSK) = \tfrac{1}{2} V_m^2 = const. \quad (1)$$

This would allow a further relative distance between the receiver and transmitter coils (d_r) or a smaller transmitted power, which is important since the maximum allowable tissue exposure to electromagnetic power is limited in biomedical devices [16]. Conversely, the power fluctuations due to ASK modulation impose additional power regulation and filtering challenges especially when the modulation index is high [11].

The superior robustness against various noise sources and interference of FM over AM has been known since the early stages of radio engineering. This fact is even more significant in

inductively powered devices, which receive data and power from the same carrier. When all other parameters are constant, the induced voltage across the receiver coil is inversely proportional to the third power of the coils relative distance ($1/d_r^3$) [1]. This means that the induced signal amplitude, which is the information carrying entity in ASK systems, is extremely sensitive to d_r and is prone to patient movements (motion artifacts) in biomedical implants or hand vibrations in RFID tags and smartcards. Even when d_r is constant, since the received power is also constant (V×I), any changes in the wireless chip current consumption, due to digital circuitry current impulses for example, directly results in voltage variations and deteriorates the quality of the received ASK signal [11]. In FSK systems on the other hand, it is very unlikely that d_r or current variations would affect the frequency of the induced signal.

In ASK modulation, the transmitter and receiver tank circuits should have high quality factors (Q) centered at the carrier frequency to get enough amplitude variations for data detection. In the proposed FSK modulation protocol however, the wireless link pass-band is centered between f_0 and f_1 with a low Q to pass enough power at both carrier frequencies (Fig. 8b). This is another advantage for the FSK technique, because in the applications of interest the quality factor of the miniature receiver coil is inherently low, particularly when the implant receiver coil is integrated and its high resistivity is unavoidable [10], [17].

Synchronization of the receiver with the transmitter is, however, easier in ASK systems. The receiver chip internal clock signal can be directly derived by stepping down the constant ASK carrier frequency [11], [10], [17]-[19]. In phase-coherent FSK, where the carrier frequencies (f_0 and f_1) have a fixed phase at the onset of every bit, an internal clock with a constant frequency can be derived from a combination of the two carrier frequencies based on the FSK modulation protocol. In non-coherent FSK, where the carrier phase is random, the timing information

should be encoded within the data stream by using self clocking schemes such as Manchester or Miller. The first option was utilized in the proposed FSK protocol with a non-return-to-zero (NRZ) data stream to achieve a higher data-rate.

To maximize the data-rate to carrier-frequency ratio, a phase-coherent protocol was devised for the FSK data transfer with data-rates as high as f_1, where f_0 is twice as f_1. In this protocol, logic "1" is transmitted by a single cycle of the carrier f_1 and logic "0" is transmitted by two cycles of the carrier f_0 as shown in Fig. 1. The carrier frequency switches at a small fraction of a cycle and only at negative-going zero crossings. This leads to a consistent bit length of $1/f_1$ and maximum data rate of f_1 bits per second. As a result, if we consider the average carrier frequency to be $f_{avr} = (f_0+f_1)/2$, then the data-rate to carrier-frequency ratio can be as high as 67%. It is also useful to notice that any odd number of consecutive f_0 cycles in this protocol is an indication of data transfer error.

Either active or passive reverse telemetry can be used in any of the aforementioned applications to send information back from the wireless chip to the transmitter. In the active reverse telemetry, a transmitter with a separate antenna, which usually works at a higher frequency, is implemented on-chip. In passive reverse telemetry, the receiver coil loading (load modulation) or capacitive tuning is changed based on the feedback information and the effects of these changes are sensed at the transmitter coil [9]. Using the carrier frequency variations for forward data transfer facilitates use of the carrier amplitude variations for reverse telemetry. Reverse telemetry is out of the scope of this paper, however, any of these methods can be incorporated with the proposed FSK modulation technique to provide a half or full duplex communication between the two parts of the wireless system.

III. FSK DEMODULATION CIRCUITS

Common FSK demodulation techniques such as FM discriminator, phase locked loop, or quadrature detector circuits need some kind of analog filtering down the signal path, which would consume a large chip area in the low-end RF applications of interest. Therefore, the received FSK carrier was treated as a base-band signal to eliminate any type of mixing or filtering. The data detection technique used here for FSK demodulation is based on measuring the period of each received carrier cycle, which is the information carrying entity in FSK modulation scheme. If the period is higher than a certain value, a logic "1" bit is detected and otherwise a logic "0" bit is received. Fig. 2 shows the FSK demodulator block diagram. A clock recovery (or regenerator) block squares up the sinusoidal carrier across the receiver tank circuit (CK_{in}) and feeds it into the data detector block which discriminates between the short (f_0) and long (f_1) carrier cycles. Finally a digital block generates the serial data bit stream and a constant frequency clock to sample the data bits.

A. Analog FSK demodulation

A simple method for time measurement in analog circuits is charging a capacitor with a constant current source and monitoring its voltage. Charging and discharging of this capacitor should be synchronized with the FSK carrier signal. If the capacitor voltage is higher than a certain value, a logic "1" bit is detected and otherwise a logic "0" bit is received. The referenced differential FSK demodulator (RDFSK) that is proposed here is based on charging a single capacitor and comparing its voltage with a constant reference voltage as shown in Fig. 1 [22].

Fig. 3 shows the clock recovery circuit which is a cross-coupled differential pair directly connected to the receiver coil nodes as shown in Fig. 2. Utilization of a positive feedback in this

circuit helps generating sharp output CK_{in} edges, which are necessary for precise timing of the carrier cycles. Fig. 4 shows a simplified schematic diagram of the RDFSK demodulator. Both S_1 and S_2 switches are controlled by CK_{in}. When CK_{in} is low, S_1 switch is closed and S_2 is open. Therefore, I_C current source linearly charges the capacitor C. During a logic "1" long cycle, C is charged up to V_1, which is twice as V_0 when a logic "0" short cycle is being received. A hysteresis comparator compares the capacitor voltage with a constant 1.26V bandgap reference voltage. The hysteresis window width, W_{hyst}, is set somewhere between V_1-V_{ref} and V_0-V_{ref}. Therefore, the comparator output switches to high during a logic "1" long cycle but not during a logic "0" short cycle. The S_2 switch discharges the capacitor in a fraction of the carrier 2nd half cycle, when CK_{in} is high; meanwhile, S_1 is open to reduce power consumption.

The output of the RDFSK data detector block, called FSK, is only a series of pulses, which discriminate between long and short FSK carrier cycles. So it cannot be directly regarded as the received data bit stream. These pulses are fed into a digital block along with CK_{in} to generate the serial data output (*Data-Out*) and constant frequency clock (*Clock-Out*). Fig. 5 shows the schematic diagram of the digital block. On every rising edge of the CK_{in}, a 2-bit shift register shifts in the FSK pulses. Every 2 successive short cycles should be regarded as a "0" bit on *Data-Out* and every single long cycle indicates a "1" bit. Any odd number of short cycles is an indication of error according to the FSK protocol and activates the error flag. To generate a constant frequency clock, a T flip-flop indicates the number of successive zeros and another T flip-flop toggles on every long CK_{in} cycle or two successive short CK_{in} cycles. The resulting clock frequency is constant at $f_1/2$ irrespective of the data contents. This is an asynchronous design to minimize the number of gates and consequently the circuit area. Therefore, signal

timings were considered carefully and delay elements were added, before the *Clock-Out* buffer for example, to avoid metastable operation of the following digital circuitry.

To verify the performance of the RDFSK demodulator, post-layout simulation was performed by choosing f_1 and f_0 equal to 4MHz and 8MHz, respectively. Fig 6 shows the resulting waveforms of this simulation. The data bit-stream of "0000111100110011" {1} is modulating the sinusoidal carrier {2} which is squared up by the clock recovery block (Fig. 3) to generate CK_{in} {3}. The capacitor and reference voltages {4} are the inputs to the hysteresis comparator, which outputs FSK pulses {5}. The FSK pulses {5} and CK_{in} {3} are the inputs to the digital block (Fig. 5), which in turn generates the output data bit-stream (*Data_Out*) {6} and a synchronous constant frequency clock (*Clock_Out*) {7}. It should be noted that since the output clock-rate is $f_1/2$, the data values should be read at both rising and falling edges of the *Clock-Out* signal {7}.

B. Digital FSK demodulation

In a digital approach for FSK demodulation, we measure the duration of carrier cycles with a constant-frequency clock time-base (f_{TB}) at a rate several times higher than the carrier frequency [23]. Most often this internal clock, which does not need to be synchronized with the carrier, is already available in the system for running other digital blocks such as a microprocessor. An *n*-bit counter runs while the carrier is "positive" and measures half of a carrier cycle. When the carrier goes "negative", the counter stops and a digital comparator decides whether a long or short carrier cycle is received by comparing the count value with a constant reference number. Then it resets the counter for measuring the duration of the next cycle.

It is necessary for the time-base period ($1/f_{TB}$) to be smaller than the time-difference between f_0 and f_1 half-cycles to enable the demodulator to discriminate between these two frequencies. In other words f_{TB} should be chosen based on:

$$f_{TB} > \frac{2 f_1 f_0}{f_0 - f_1} \tag{2}$$

and the minimum width of the counter (n) should satisfy:

$$2^n > f_{TB}/2f_1 \tag{3}$$

In order to simplify the demodulator circuit and reduce dynamic power consumption, the digital comparator can be combined with the counter by choosing f_0, f_1, f_{TB} and n such that:

$$2^n f_0 > f_{TB} > 2^n f_1 \tag{4}$$

In this case the most significant bit (MSB) of the counter determines whether a long or short carrier cycle is received and the constant reference number is equal to 2^n.

Based on the proposed FSK modulation protocol and the required bandwidth for a visual implant, f_0 and f_1 were chosen equal to 8 and 4MHz, respectively. A lower limit for the time-base clock, f_{TB} > 16MHz, is then set by (2). By choosing $n = 3$, (4) defines a new range for f_{TB}, 64MHz > f_{TB} > 32MHz, which satisfies (2) and (3) as well. Therefore, a 5-stage ring-oscillator was designed to generate f_{TB} = 49MHz at the center of the above range to provide the maximum level of robustness. It should be noted that as long as f_{TB} is in the desired range (4), the phase noise and process or temperature-dependent frequency variations of this oscillator do not affect the demodulation procedure.

Fig. 7 shows the schematic diagram of the DFSK demodulator and Fig. 8 shows sample simulation waveforms when "00111100110011" data bit-stream {1} is FSK modulated and

applied to the DFSK demodulator circuit {2}. The clock recovery block squares up the received FSK carrier and generates CK_{in} {3}. The 5-stage ring-oscillator generates a time-base clock at f_{TB}, which runs the 3-bit counter after being gated by CK_{in} {4}. When CK_{in} is high, the counter is running, and it freezes when CK_{in} is low. The counter *MSB* stays low during short (62.5ns) carrier half-cycles when count < 4, however, it goes high during long (125ns) carrier half-cycles when count ≥ 4 {5}. The counter resets when CK_{in} goes low during the 2nd carrier half-cycle to be ready for detecting the type of the next cycle. The *MSB* signal {5} cannot be directly regarded as the received data bit stream. Therefore, these pulses are fed into the digital block (Fig. 5) along with CK_{in} {3} to generate *Data-Out* {6} and *Clock-Out* {7}.

IV. Wideband Inductive Link

Detailed design of the inductive link for biomedical implants is described in [1]-[3]. Almost all of these inductive links are designed for narrowband carrier signals, which is not the case in the proposed FSK modulation scheme. The main problem with a narrow bandwidth in high-speed FSK data transfer is inter-symbol interference, which is caused by the residual ringing that distorts the received carrier signal when the transmitter switches from one frequency to another. The Carlson's rule approximates the necessary bandwidth (*BW*) to include 98% of the total power of an FM signal [24]:

$$BW \approx 2(\delta_{\max} + f_{i\max}) \tag{5}$$

where δ_{max} is the maximum frequency shift caused by modulation and f_{imax} is the maximum frequency content of the modulating signal. In the proposed FSK protocol, $\delta_{max} = f_1/2$ with respect to f_{avr} and the maximum data rate of f_1 can be considered as a square waveform at $f_1/2$. Therefore, the main lobe of data spectrum has a maximum frequency of $f_{imax} = f_1$. By substituting

these values in (5), a bandwidth of $BW \approx 3f_1$ is needed to include 98% of the FSK carrier power. However, it should be noted that contrary to the analog FM, here the goal is not a direct reconstruction of the data waveform, but correct detection of the data values. The experimental measurements show that an inductive link with half of the estimated bandwidth ($1.5f_1$) can still provide an acceptable bit error rate (BER) in a system equipped with error detection circuitry.

The easiest way to increase the inductive link bandwidth is to lower the quality factor (Q) of the transmitter and receiver tank circuits by adding resistive components. However, the resulting increase in power dissipation especially in the implantable side is not desirable. Another method is to modify the transmitter output spectrum by adding two zeros at f_0 and f_1, where the peaks of the FSK carrier spectral power are located. Fig. 9a shows a simplified schematic diagram of the modified inductive link. The external parts of the system are replaced with an AC source and a source resistance (R_s), whereas the implant is replaced by a resistive load (R_L) and its parasitic input capacitance (C_{in}). A combination of both series and parallel LC-tank circuits are used to generate two zeroes across the FSK source output nodes at f_0 and f_1. It can be shown analytically that this condition will be satisfied if L_S-C_S and L_P-C_P are chosen such that:

$$\frac{1}{2\pi\sqrt{L_P C_P}} = \frac{1}{2\pi\sqrt{L_S C_S}} = \sqrt{f_0 f_1} = f_m \quad \text{and} \tag{6}$$

$$\frac{1}{2\pi\sqrt{L_S C_P}} = f_1 \quad \text{and} \tag{7}$$

$$\frac{1}{2\pi\sqrt{L_P C_S}} = f_0 \tag{8}$$

In this series-parallel LC-tank combination, either L_P or L_S can be considered as the transmitter coil (L_t). The effect of the receiver coil (L_r) and its loading (C_r, C_{in}, and R_L) is neglected in the above calculations, because the mutual coupling between the two coils (M) is

usually very small [1]. Fig. 9b shows the simulated spectrums of V_{FSK} and V_r, the voltages across the FSK source output and the receiver coil, when the circuit parameters are chosen based on Table 1. It can be seen that the zeros at f_0 and f_1 have provided a -3dB bandwidth of about f_1 across L_r without any additional resistive components. The time-domain waveform of the received FSK carrier signal (V_r) in Fig. 9c shows that the carrier frequency switches immediately with no residual ringing. Fig. 9c also shows that f_0 and f_1 are suppressed at the FSK source output (V_{FSK}) and there are only spikes at the frequency switching points due to the other unsuppressed frequency components that become significant at these points.

V. Measurement Results

The RDFSK and DFSK demodulators were included along with a CMOS full-wave rectifier [25] in a prototype chip for a wireless stimulating microsystem [21] and fabricated in the AMI 1.5-μm 2-metal 2-poly standard CMOS process, which is shown in Fig. 10 [22], [23]. The ring-oscillator generates f_{TB} = 50.5MHz at 5V supply, which is very close to the target value of 49MHz. According to (4) with this f_{TB} value, the DFSK demodulator works with FSK carriers from 3.2/6.4MHz to 12.5/25MHz.

To evaluate the overall performance of the wideband FSK wireless link, a square-shaped digital FSK signal is generated on a PC platform based on the proposed FSK protocol using a high speed digital I/O card (National Instruments DAQ-6534). The digital FSK signal passes through a band-pass filter, which rejects its DC and high frequency components and turns it into a sinusoidal FSK signal before being amplified by a wideband power amplifier (Amplifier Research 25A250A). The amplified FSK carrier is transmitted through the series/parallel LC-tank combination as shown in Fig. 9. The receiver coil, which is inductively coupled to L_P and its specifications are summarized in Table 1, receives the FSK carrier and applies it to the rectifier

and demodulator blocks: Fig. 11 shows some of the prototype chip measured waveforms when a 5/10MHz FSK carrier is used. The FSK carrier is measured differentially across the L_rC_r-tank and shown on the 3 lower traces (~$30V_{p\text{-}p}$). Even though a maximum data rate of 5Mbps (f_1) can be transmitted by a 5/10MHz carrier according to the proposed FSK protocol, it would need $BW \approx$ 7.5MHz or $1.5f_0$ according to section IV, while the inductive link can only provide $BW \approx$ 5MHz (without using dissipative components) as shown in Fig. 9b. Therefore, the data rate was reduced to 2.5Mbps by repeating every bit twice in order to reduce the required bandwidth and achieve a bit error rate of 10^{-5}. The upper two traces in Fig. 11 show the recovered clock (*Clock-Out*) and demodulated serial data bit-stream (*Data-Out*) at 2.5MHz and 2.5Mbps, respectively. To the authors' knowledge, this is the fastest data-rate ever reported in inductively coupled wireless applications [2]-[12].

Table 2 shows a comparison between measured results of the 3 demodulator circuits that were discussed in section III. All these circuits are designed to achieve the highest possible data rate without optimization in terms of power or chip area consumption. With this criterion, the DFSK circuit seems to offer the best performance. However, it should be noted that with a different set of design criteria, the optimal choice might be different. For example, if a high data rate to carrier frequency ratio is sought by using a carrier frequency in 100kHz range, then I_C in Fig. 4 can be much smaller and the RDFSK would be the most power efficient solution.

VI. SUMMARY

We have developed a high-rate FSK modulation protocol, a wideband inductive link, and two FSK demodulator circuits for wireless operation of the stimulating microelectrode arrays with over 1000 stimulating sites. This FSK modulation/demodulation technique, which has several advantages over the typical ASK method, can also be used in other inductively powered wireless

applications such as RFID tags and smartcards by adding a mechanism for reverse telemetry. A wideband inductive link between a pair of loosely coupled coils is needed to receive the FSK carrier signal across the receiver coil without significant distortion. In the demodulator circuit, a serial data bit-stream and a constant frequency clock are extracted from the FSK carrier, which is in 1~25MHz range and also powers the chip after being rectified. The RDFSK and DFSK demodulators are fabricated in the AMI 2-metal 2-poly 1.5-μm standard CMOS process, occupying areas of 0.41mm^2 and 0.29mm^2, respectively. The measurement and simulation results, which are summarized in Table 2, suggest that the DFSK demodulator is a better choice for achieving the highest data rate and process independence. However with different design criteria, the analog approach (RDFSK) might be favorable based on the system requirements.

ACKNOWLEDGEMENTS

The authors wish to thank Prof. K.D. Wise of the EECS department of the University of Michigan and Dr. W.J. Heetderks of the National Institutes of Health for their guidance. This work was done using WIMS-NSF-ERC facilities and was supported by the Neural Prosthesis Program, under contract number NIH-NINDS-N01-NS-9-2304.

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LIST OF FIGURES

LIST OF TABLES

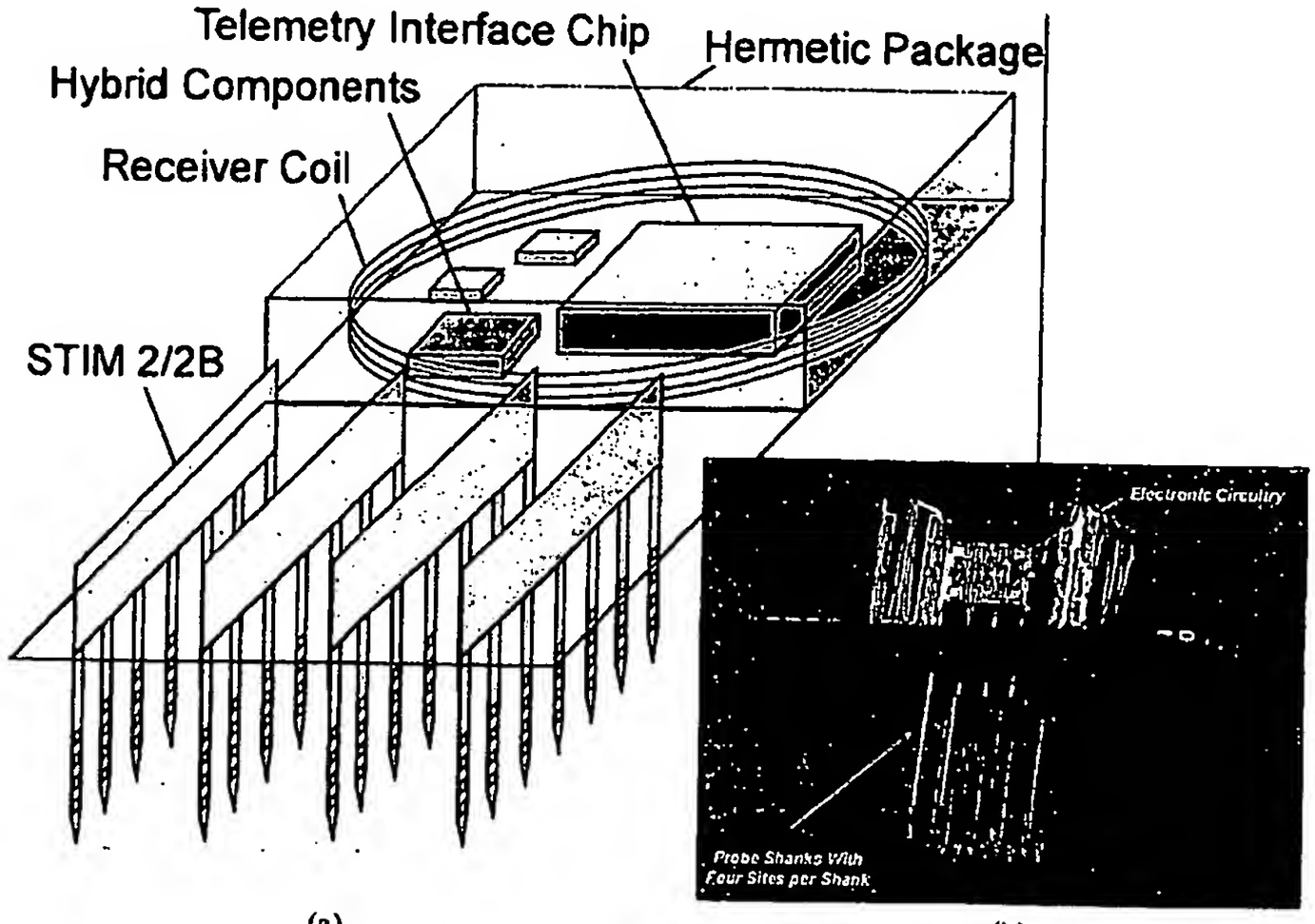


Fig. 1. (a) A wireless 3D-microstimulator array with hybrid-coil and interface chip mounted on a micromachined platform. (b) A hard-wired 3D stimulator array [7, 8].

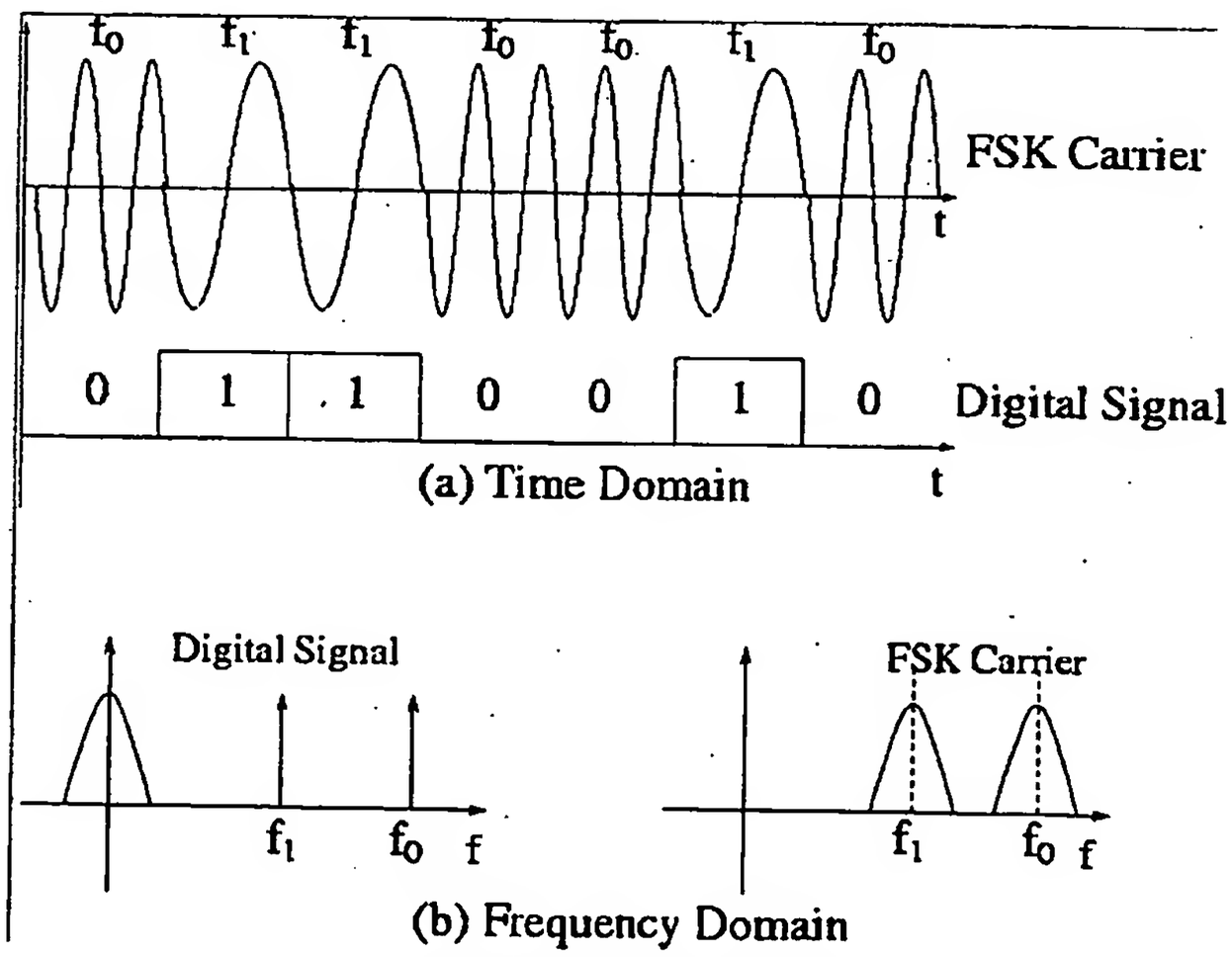


Fig. 2. Frequency shift keying in time and frequency domains.

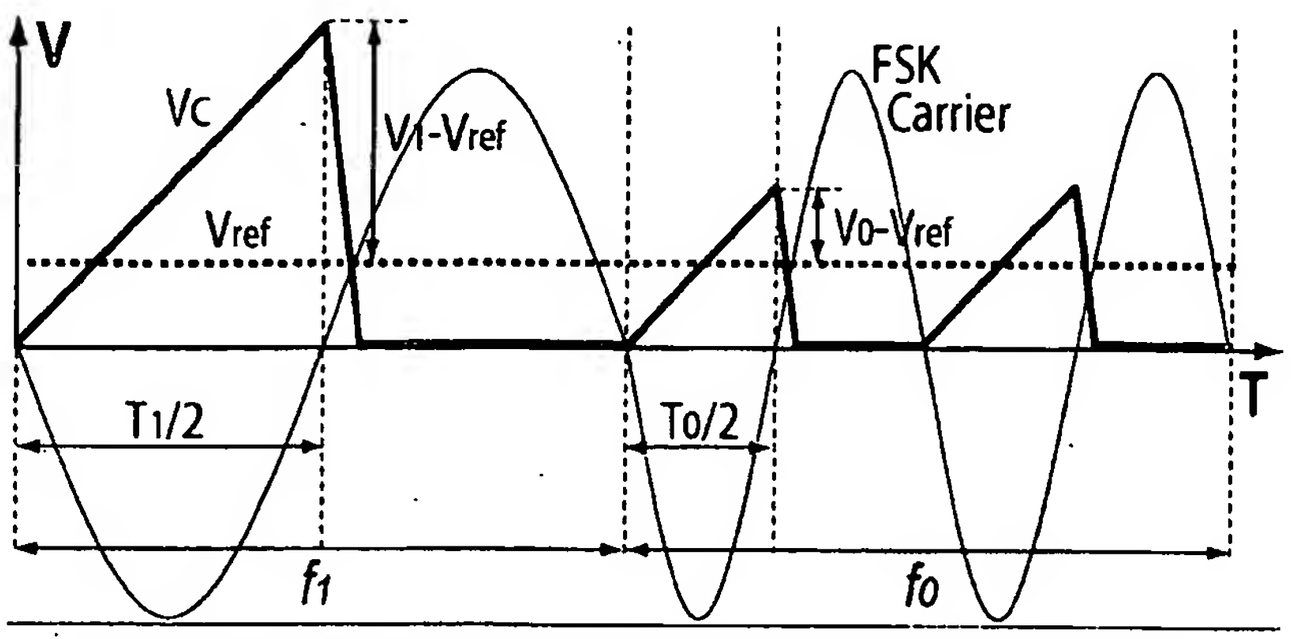


Fig. 3. The referenced differential FSK (RDFSK) data detection technique.

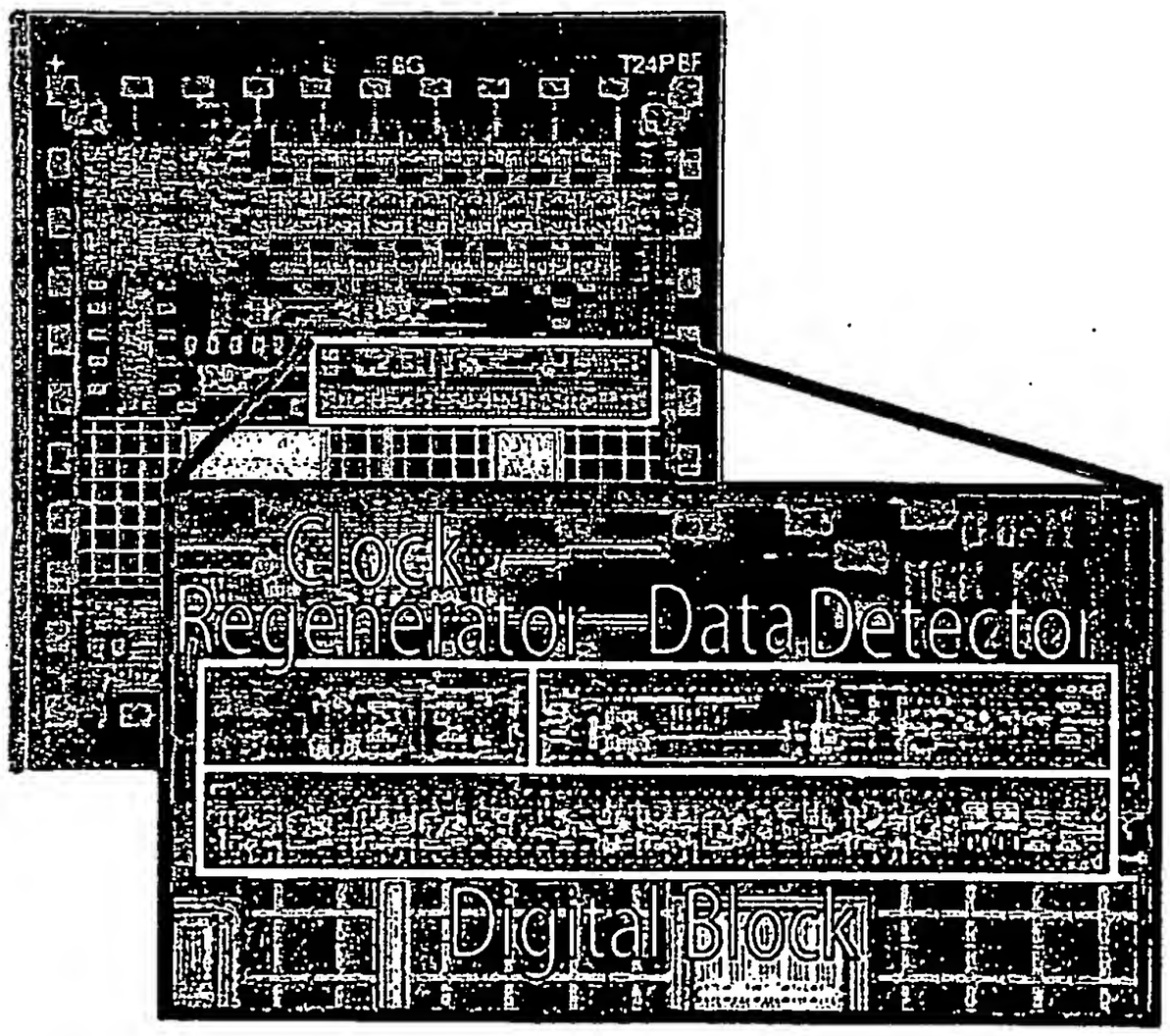


Fig. 4. The RDFSK prototype chip and its floor plan.

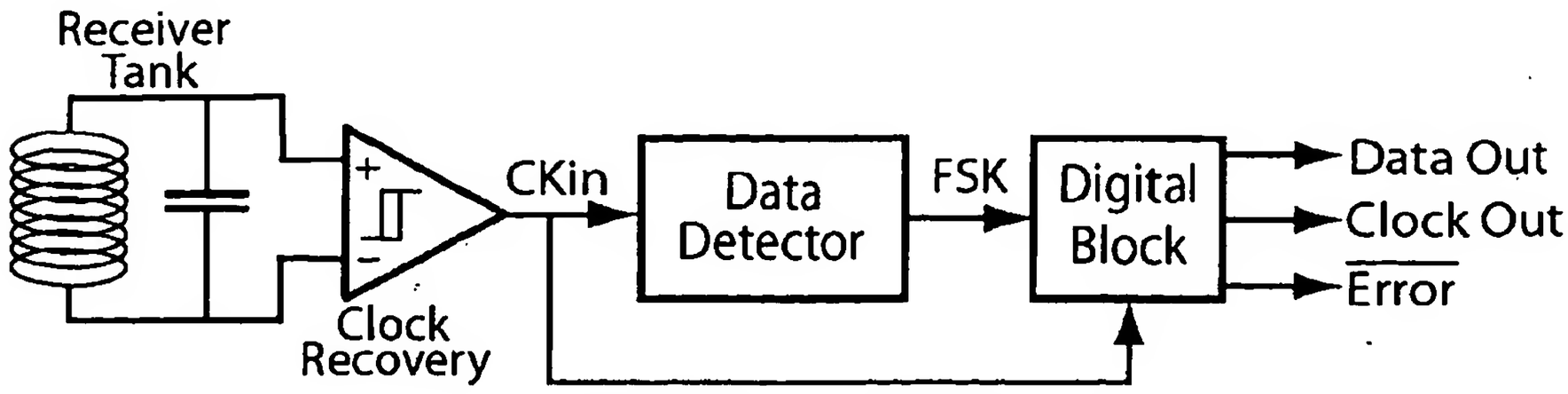


Fig. 5. The RDFSK demodulator block diagram.

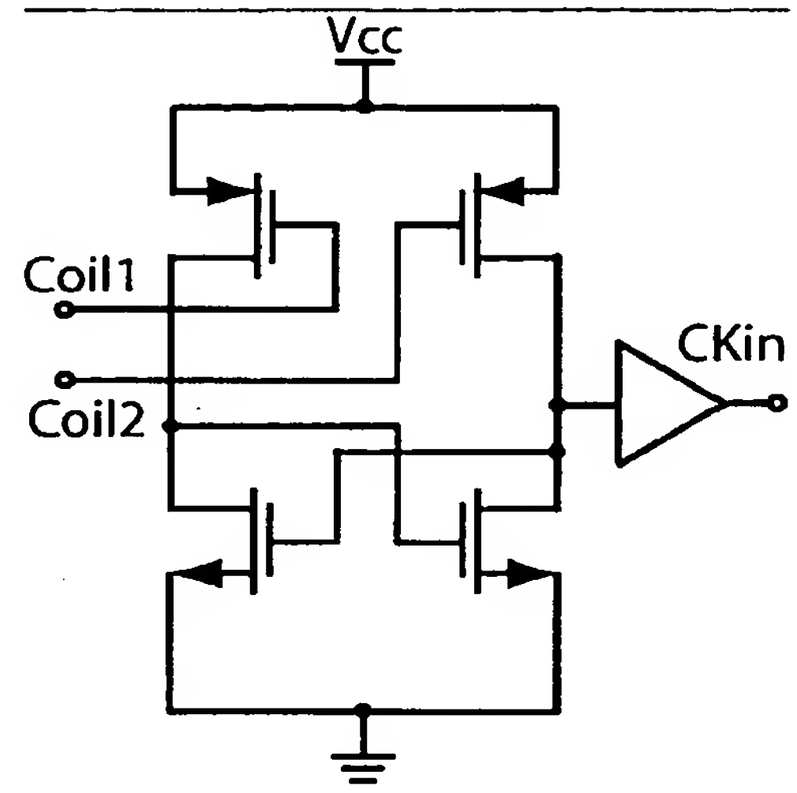


Fig. 6. The clock recovery circuit schematic diagram.

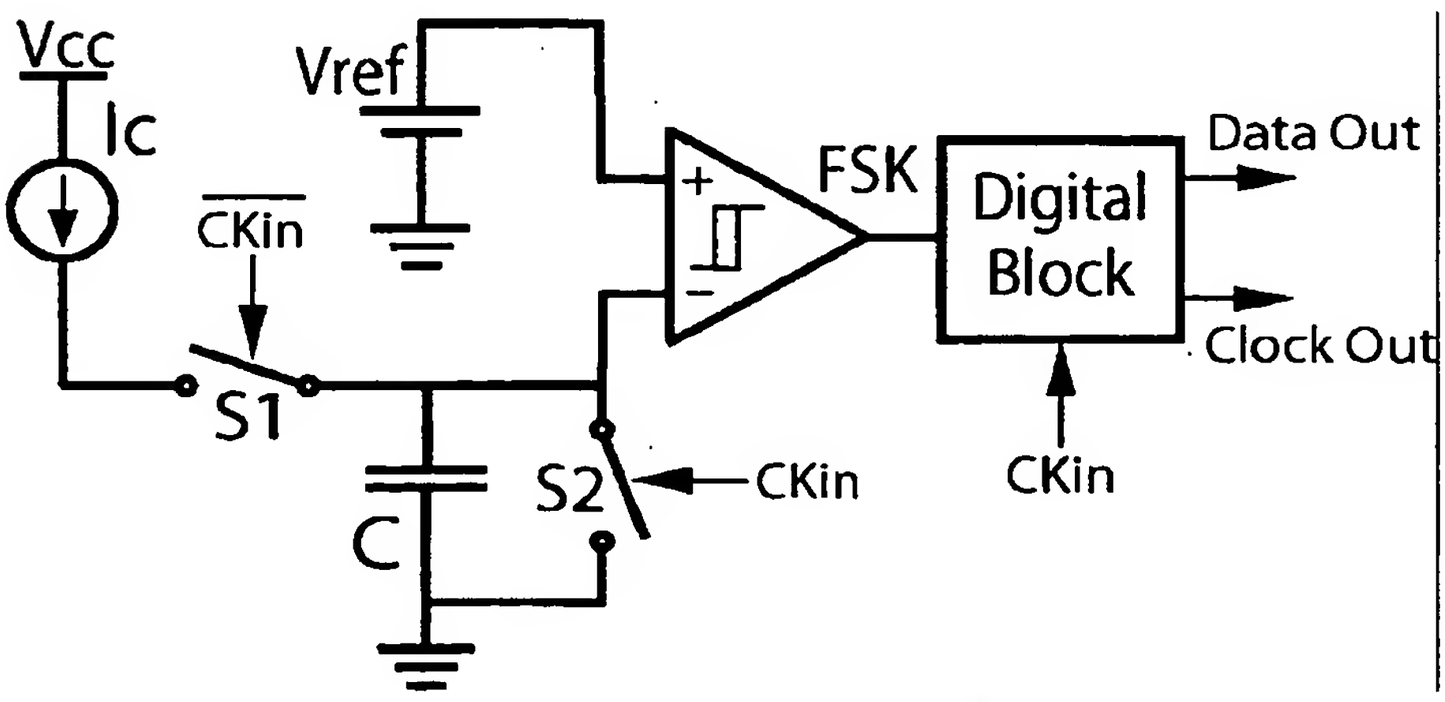


Fig. 7. The RDFSK data detector simplified schematic diagram.

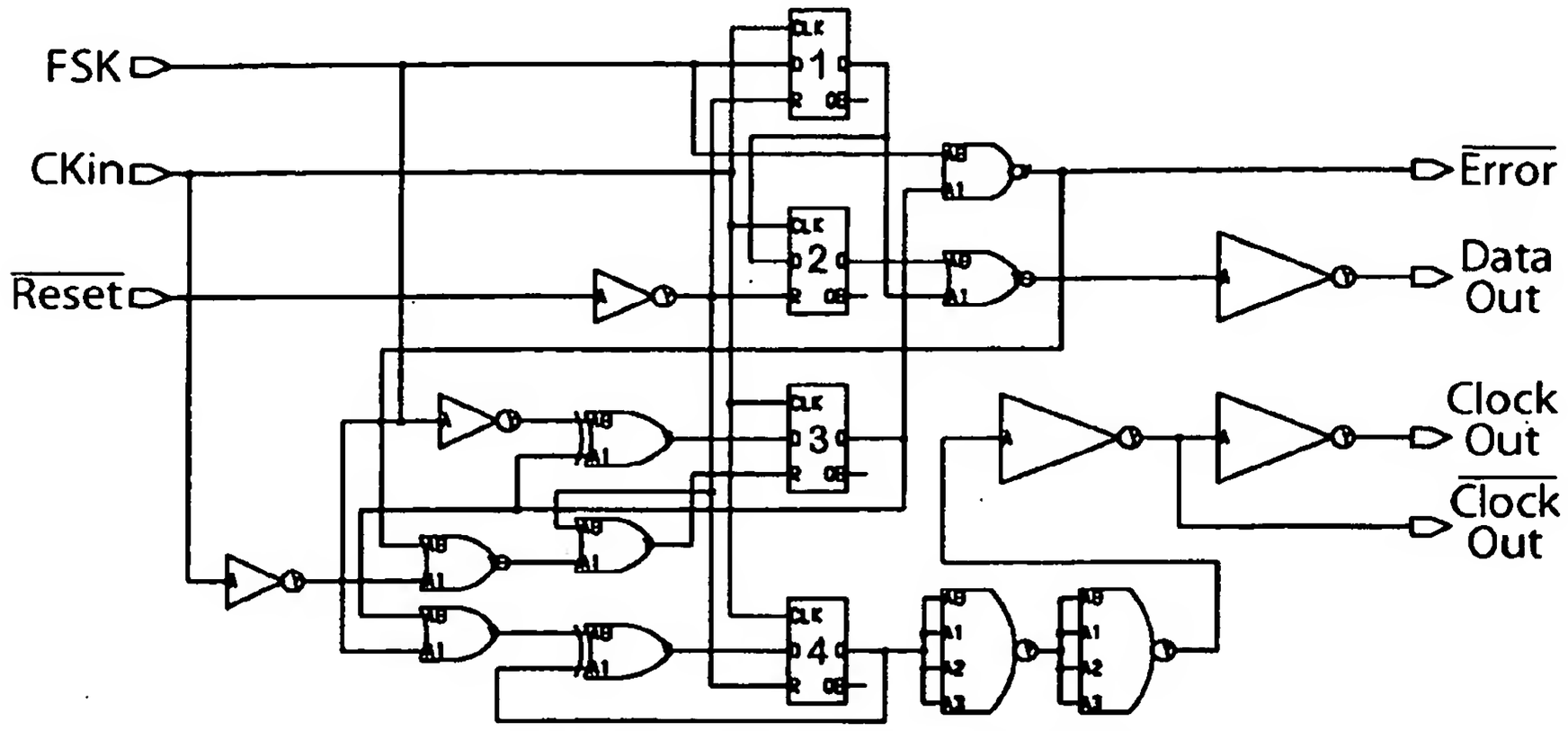


Fig. 8. The RDFSK digital block schematic diagram.

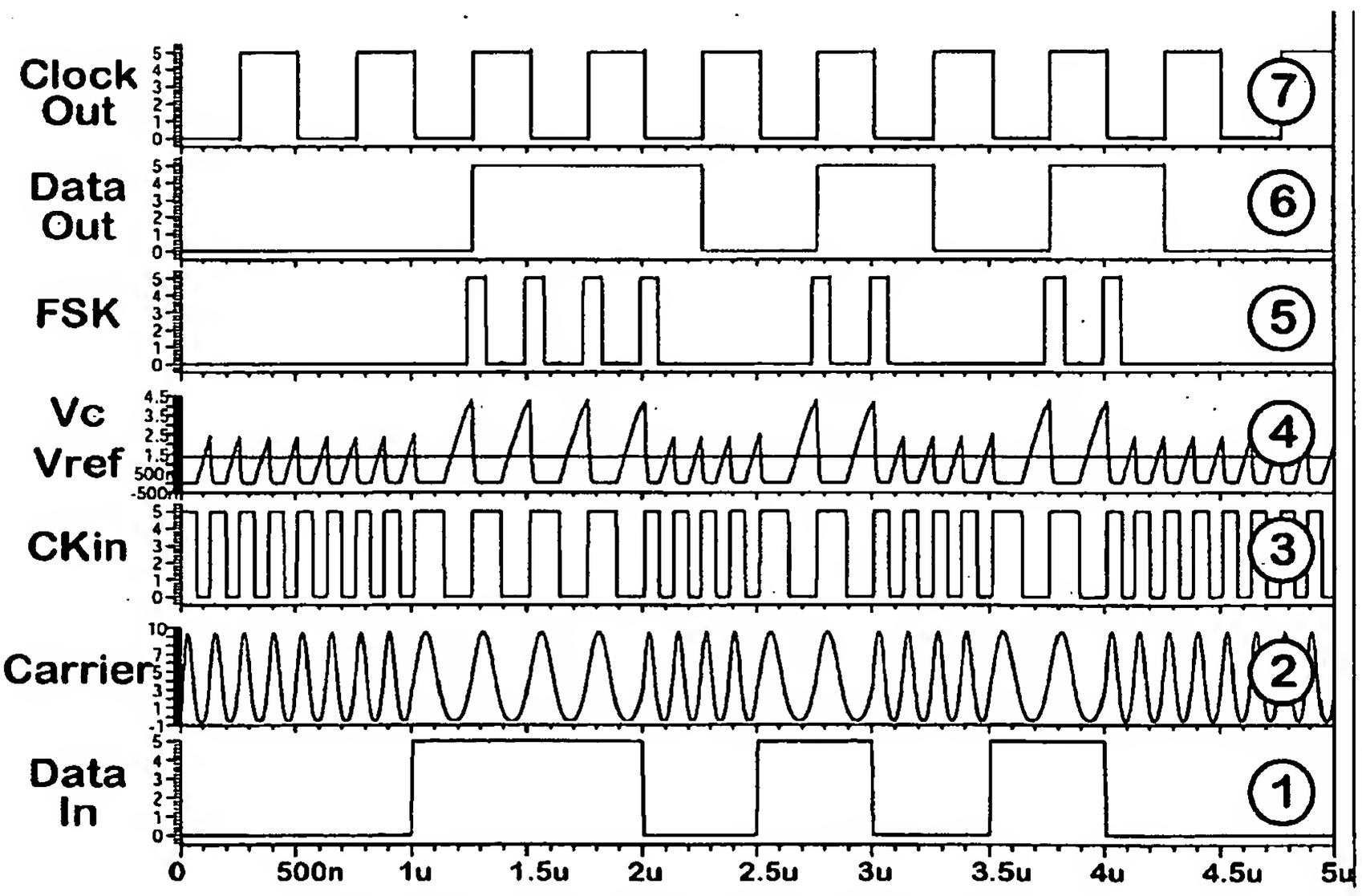


Fig. 9. The RDFSK demodulator simulated waveforms.

the authors.

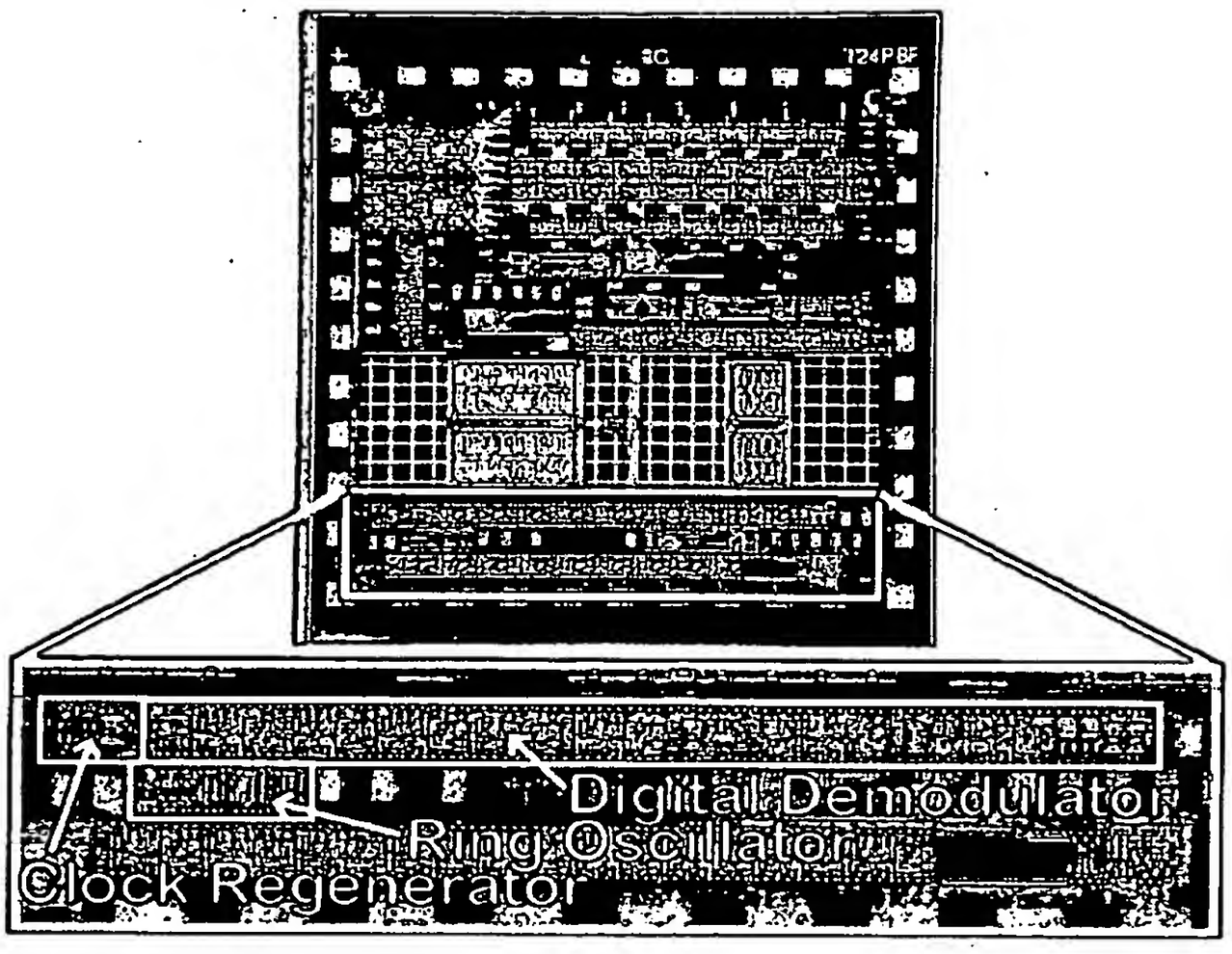


Fig. 10. The D-FSK demodulator prototype chip and its floor plan.

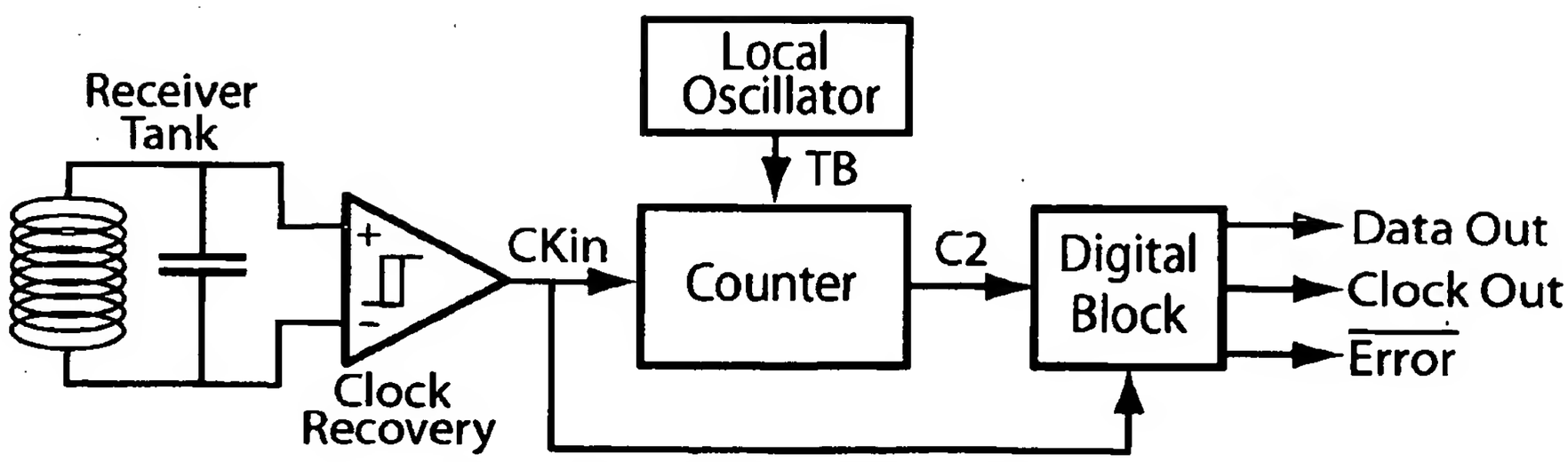


Fig. 11. The D-FSK demodulator block diagram.

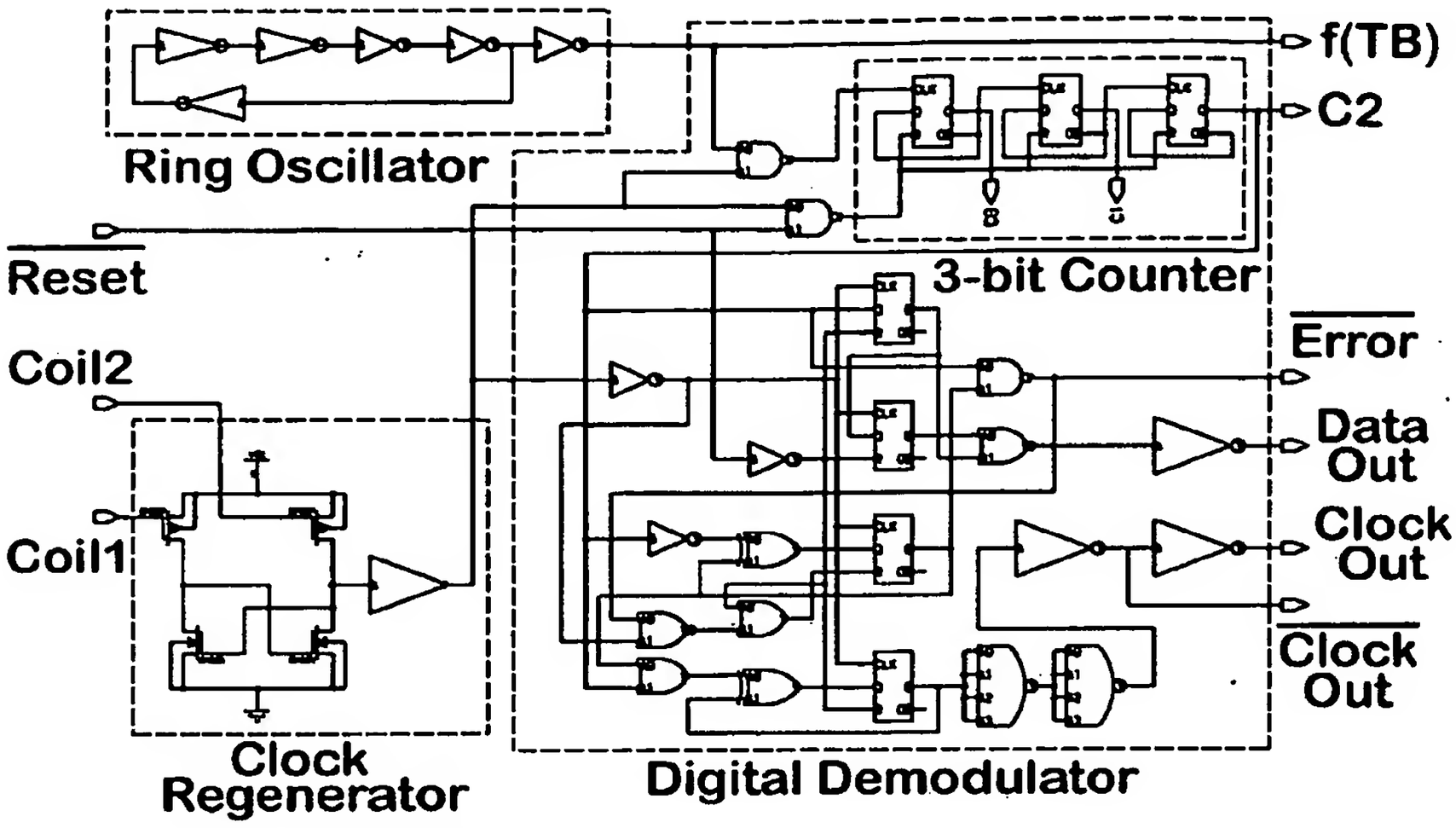


Fig. 12. The D-FSK demodulator schematic diagram.

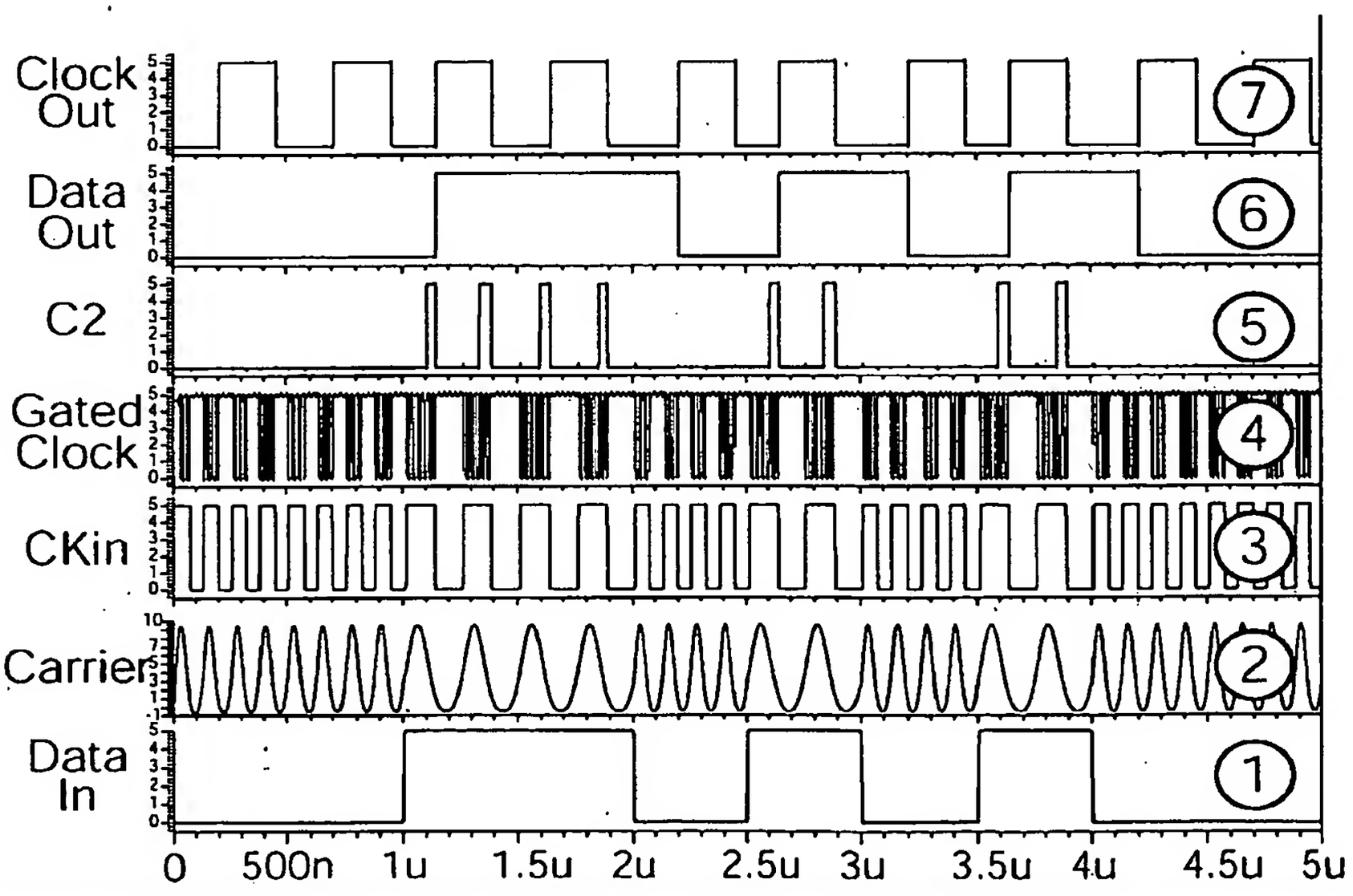


Fig. 13. The D-FSK demodulator simulated waveforms.

the authors.

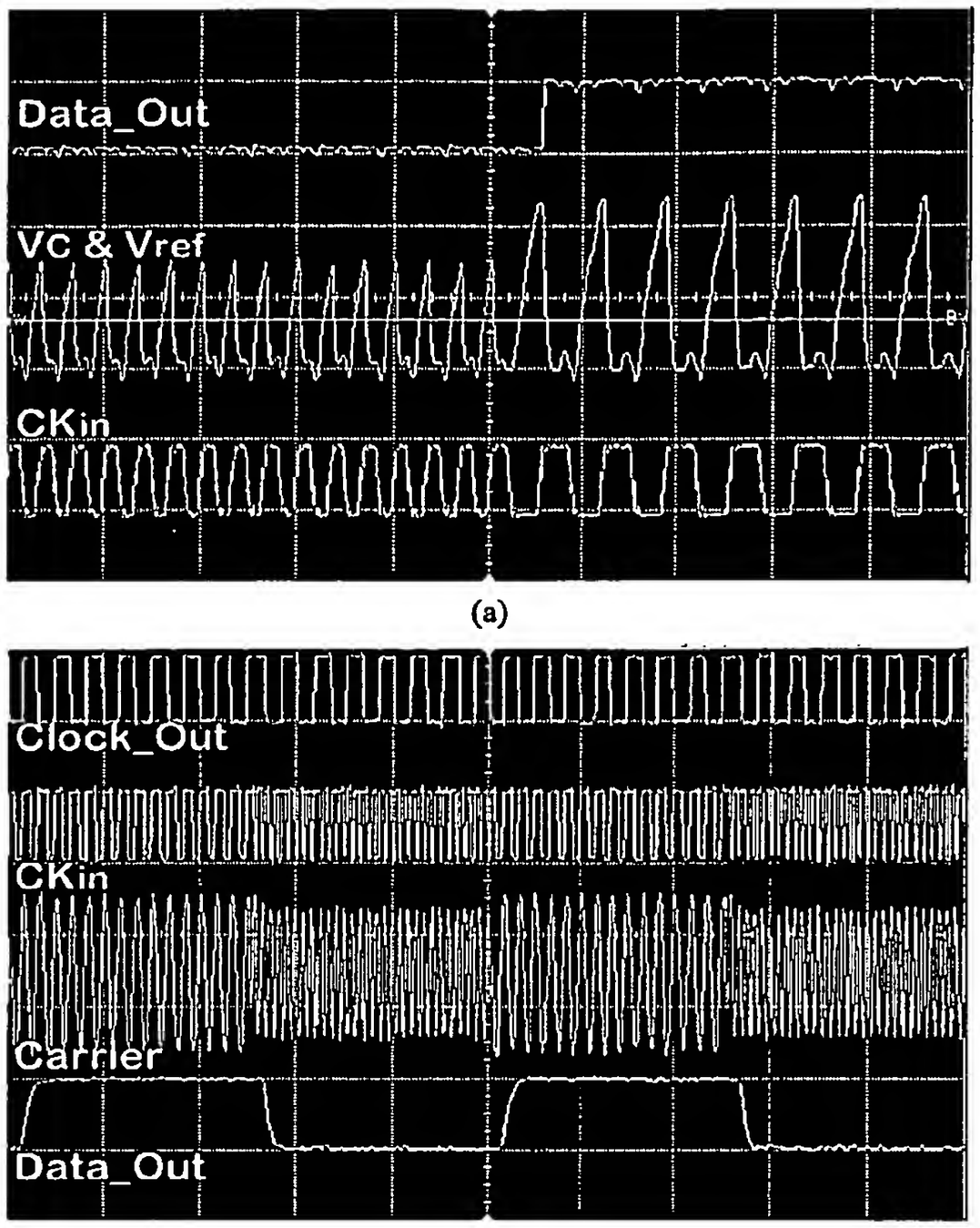
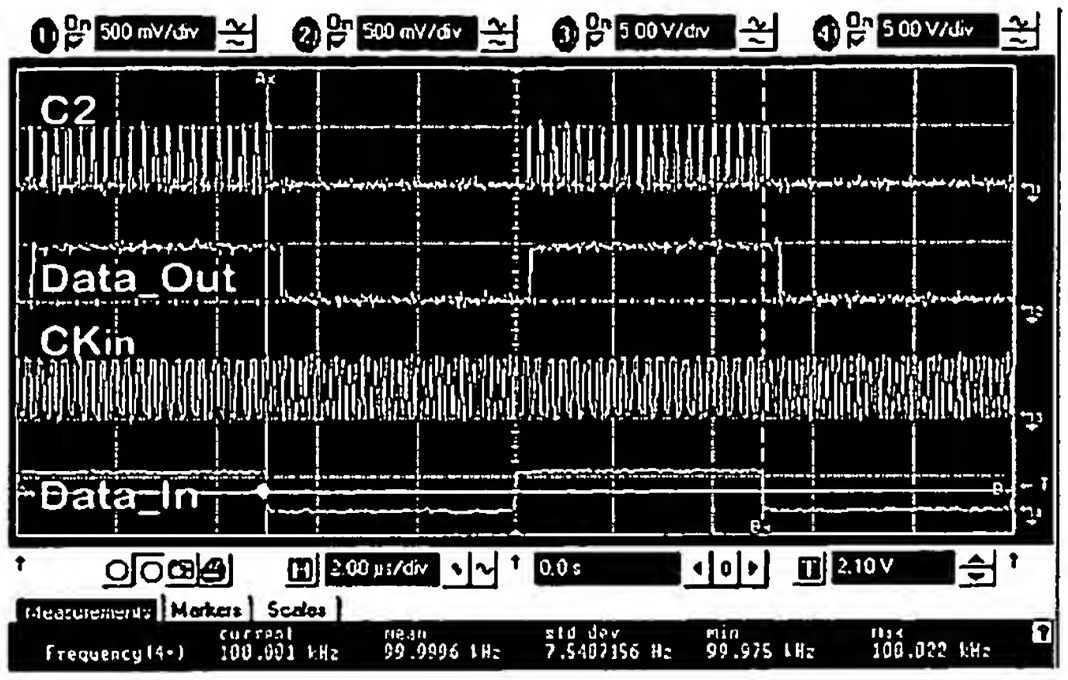
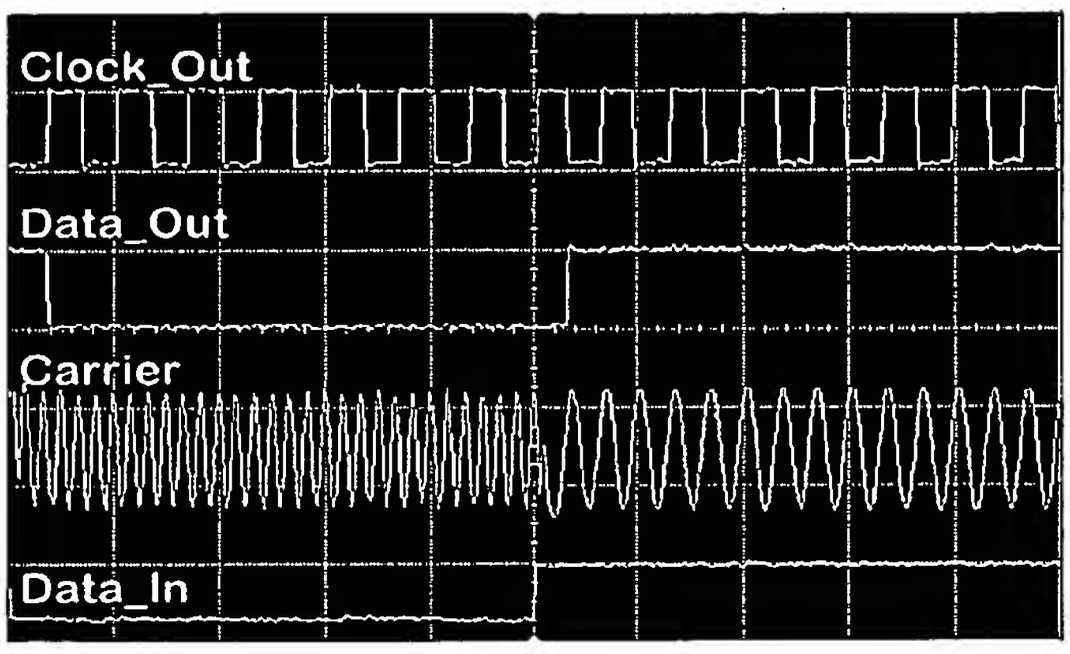


Fig. 14. The RDFSK measured waveforms at 200 Kbps with f_1 and f_0 equal to 3MHz and 6MHz respectively. From top: (a) Data-Out, V_C and V_{ref} superimposed, CK_{in} [500ns/div] (b) Clock-Out, CK_{in}, Sinusoidal Carrier input, Data-Out [2μs/div].



(a)



(b)

Fig. 15. The D-FSK measured waveforms at 200 Kbps with f_0 and f_1 equal to 8MHz and 4MHz respectively. From top: (a) Counter MSB C_2, Data-Out, CK_{in}, Data-In [2µs/div] (b) Clock-Out, Data-Out, Carrier, Data-In [500ns/div].

TABLE 1
TEST RESULTS AND SPECIFICATIONS SUMMARY OF THE TWO DEMODULATION TECHNIQUES

Demodulation Technique	**RDFSK**	**D-FSK**
Process technology	AMI 1.5-μm	AMI 1.5-μm
Die size (mm^2)	2.2 × 2.2	2.2 × 2.2
Circuit area (mm^2)	0.41	0.29
Carrier frequency range (MHz)	2 ~ 20	4 ~ 20
Maximum data rate (Mbps)	3	4
C (pF)	1.2	-
I_C (μA)	40	-
V_{ref} (V)	1.26	-
Time-base clock (MHz)	-	50.1
Counter width (n)	-	3
Supply voltage (V)	5	5
Power dissipation @ 200Kbps (mW)	0.45	0.38

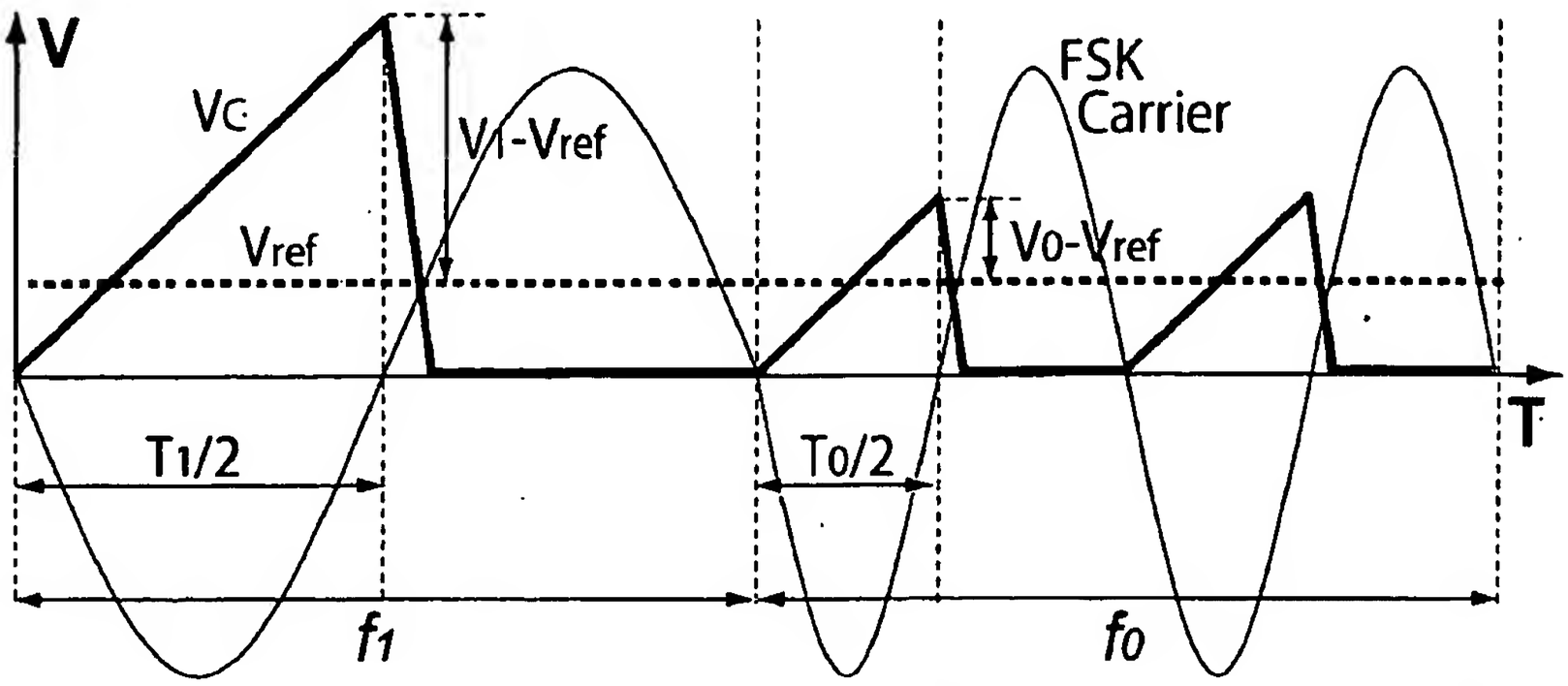


Fig. 1. The proposed FSK modulation protocol and analog Referenced Differential FSK data detection technique.

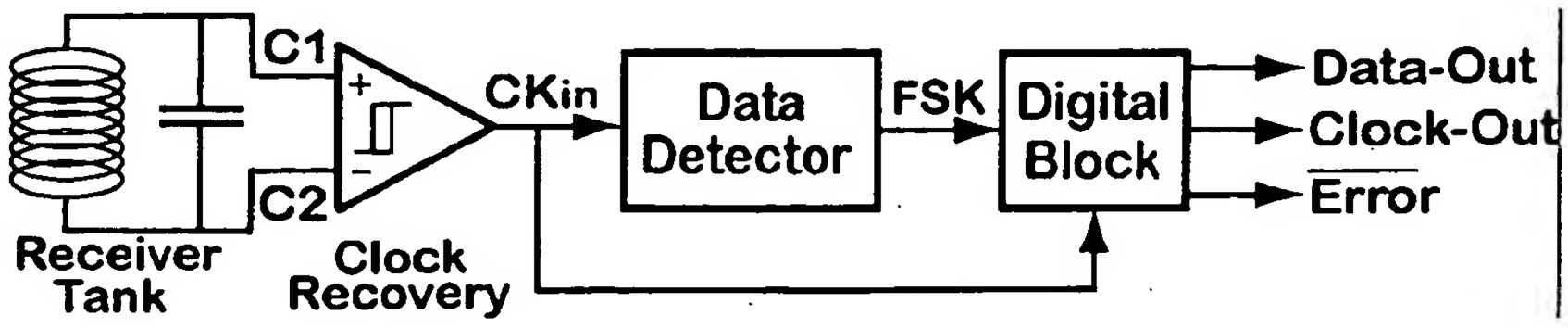


Fig. 2. The FSK demodulator block diagram.

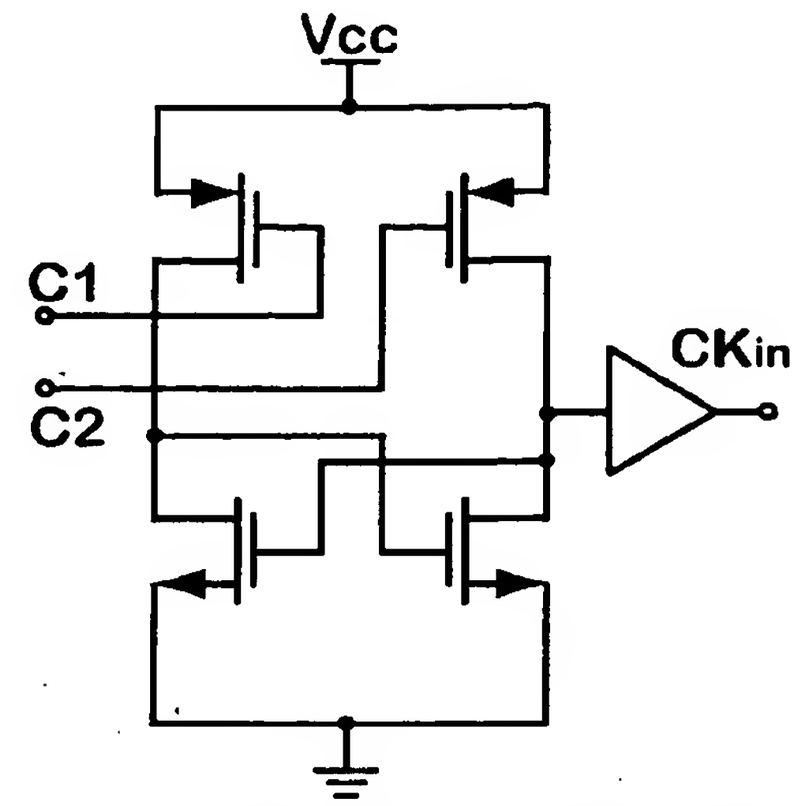
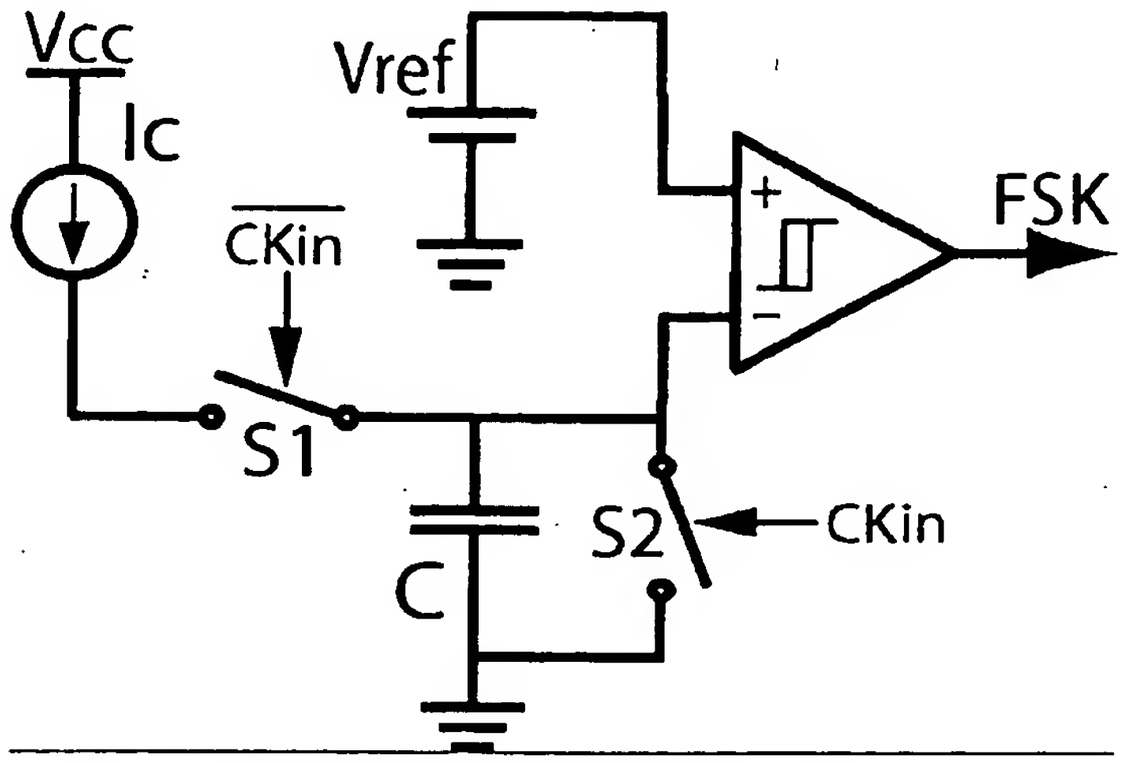


Fig. 3. The clock regenerator schematic diagram.



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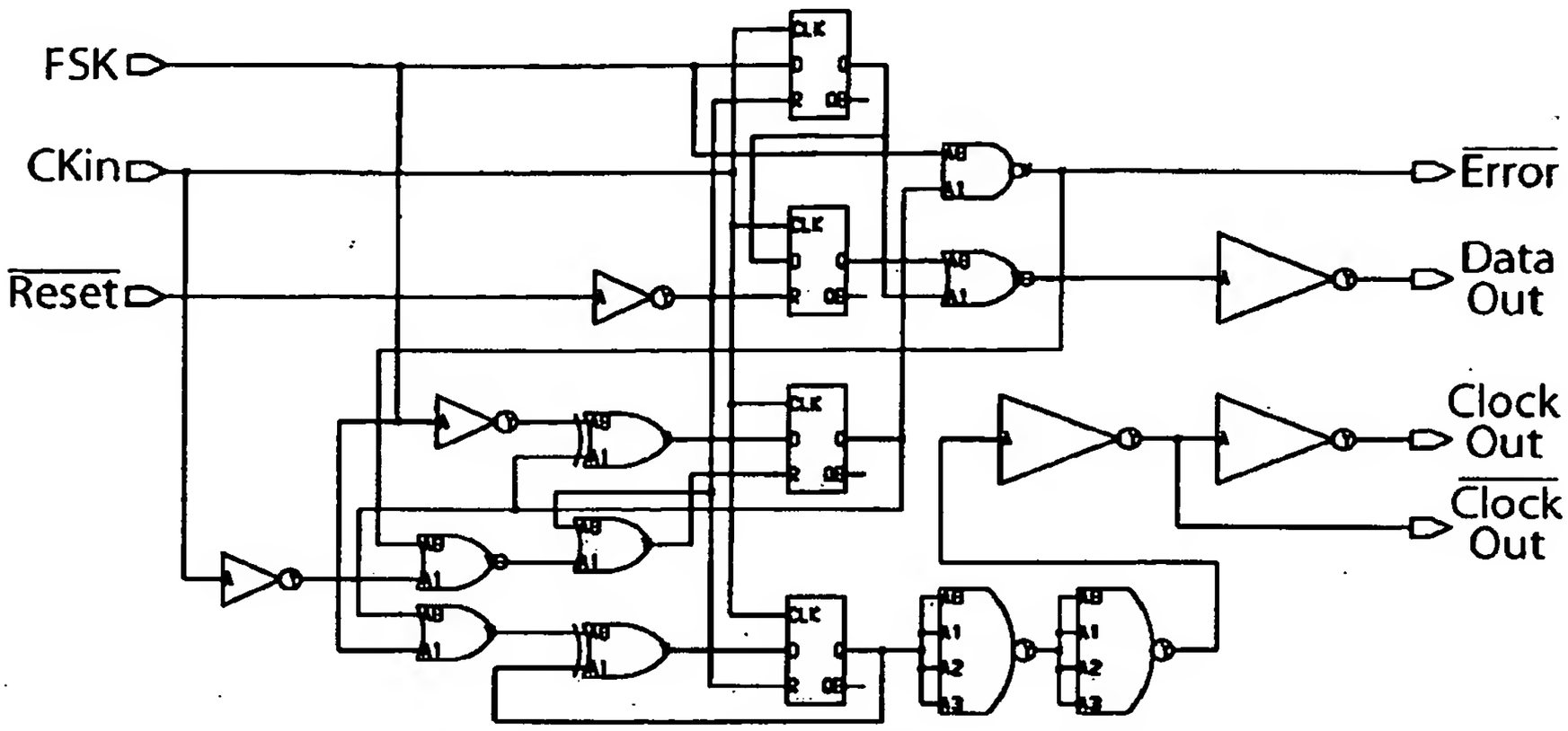


Fig. 5. The RDFSK digital block schematic diagram.

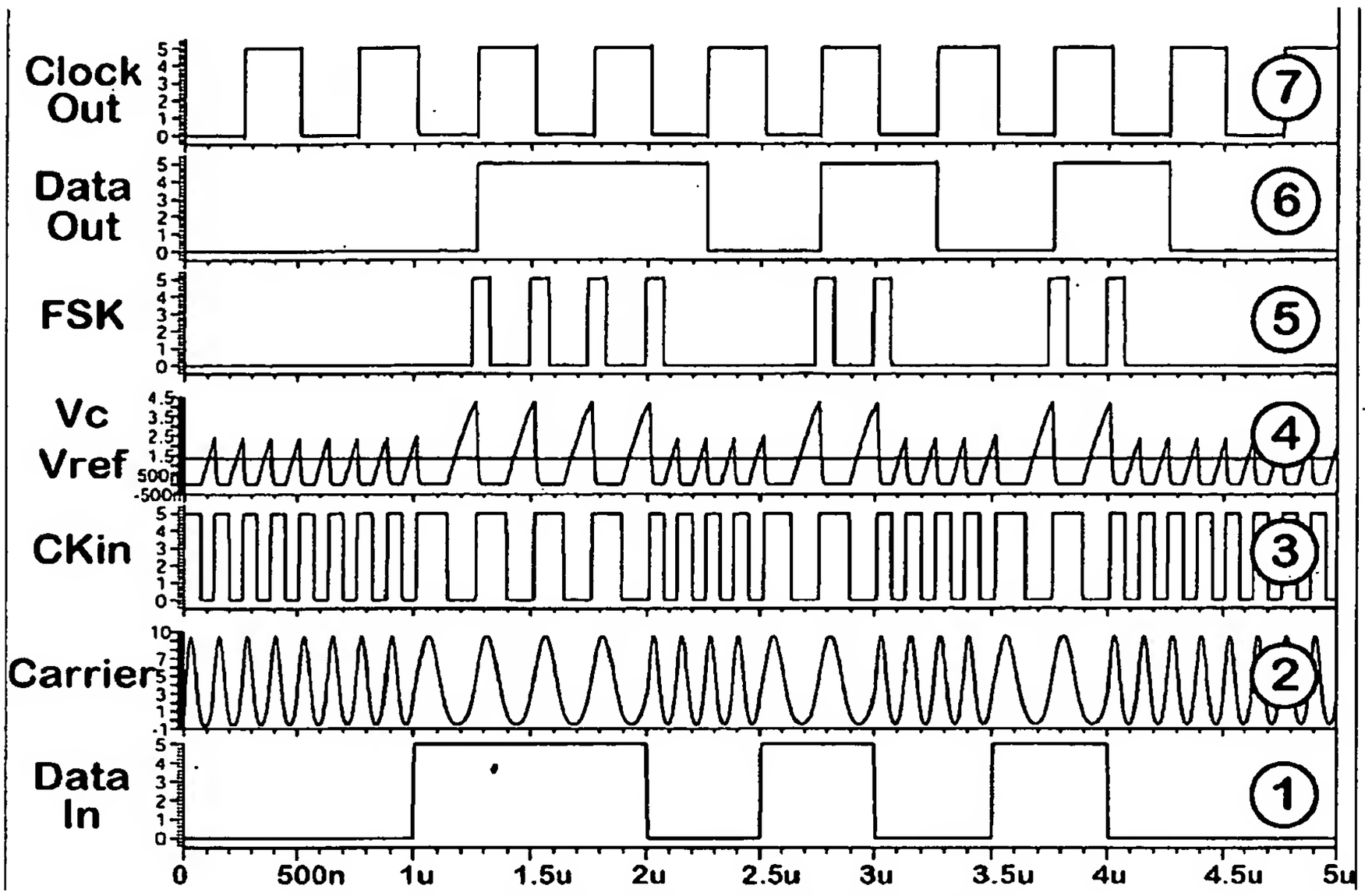


Fig. 6. The RDFSK demodulator simulated waveforms.

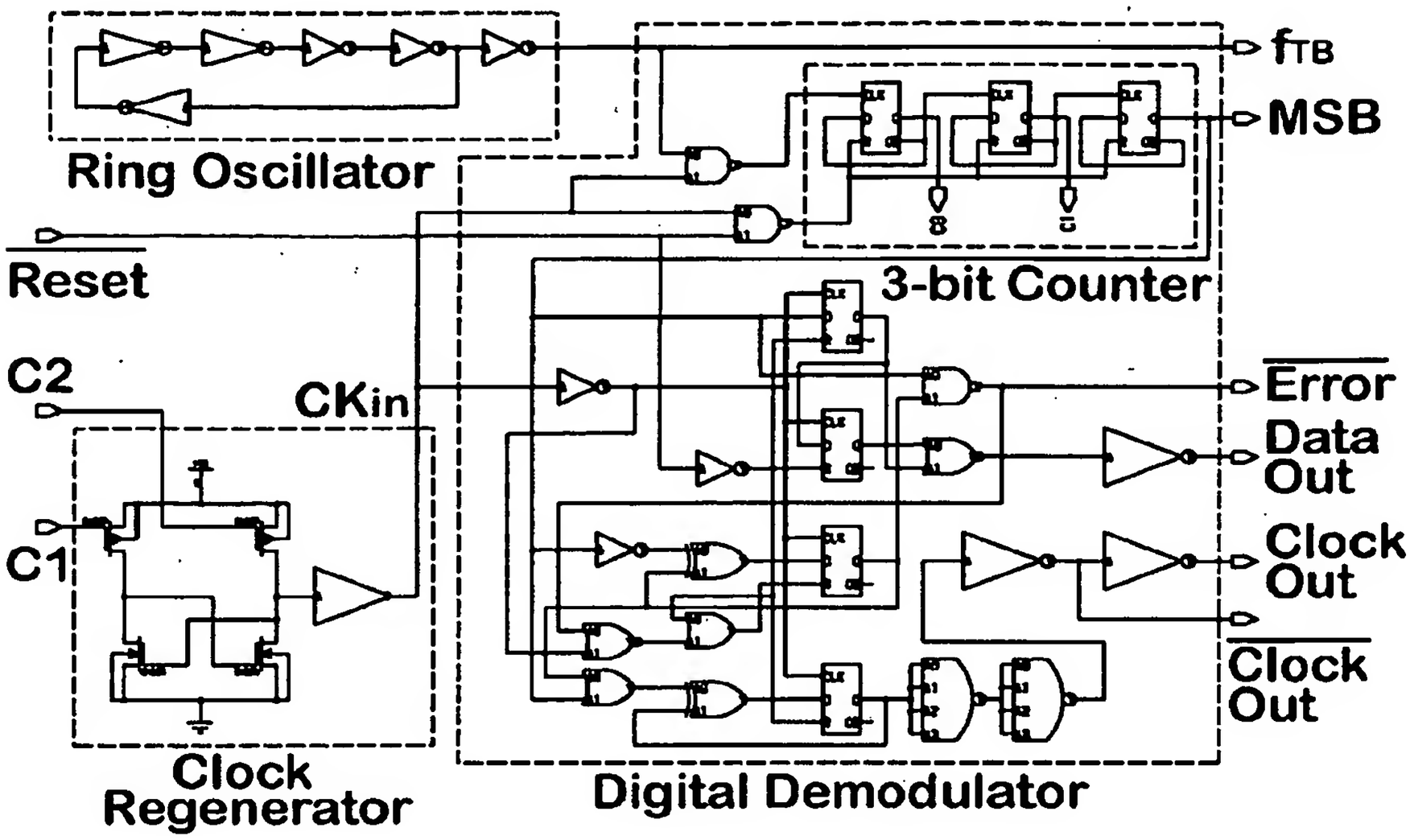


Fig. 7. The DFSK demodulator schematic diagram.

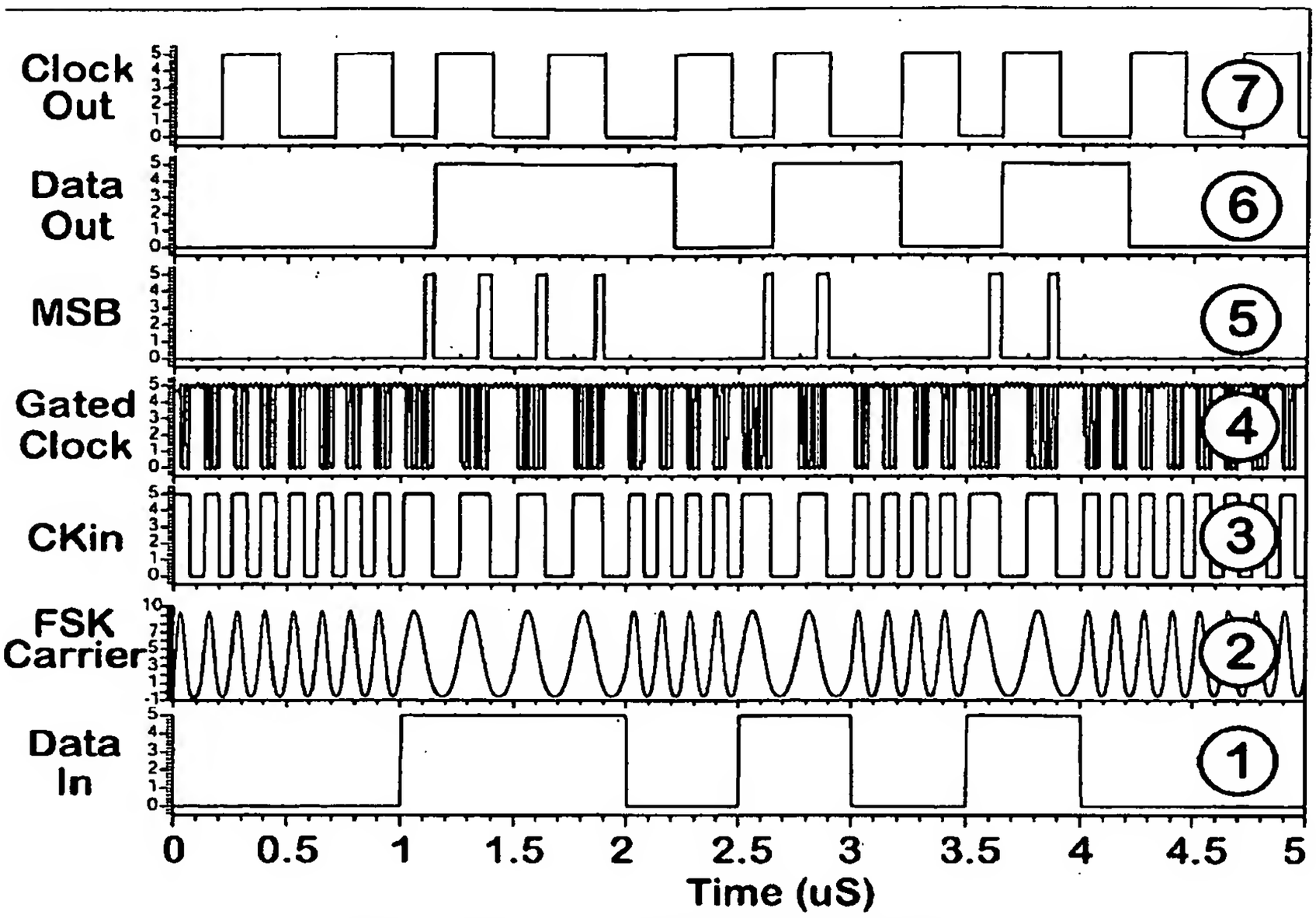
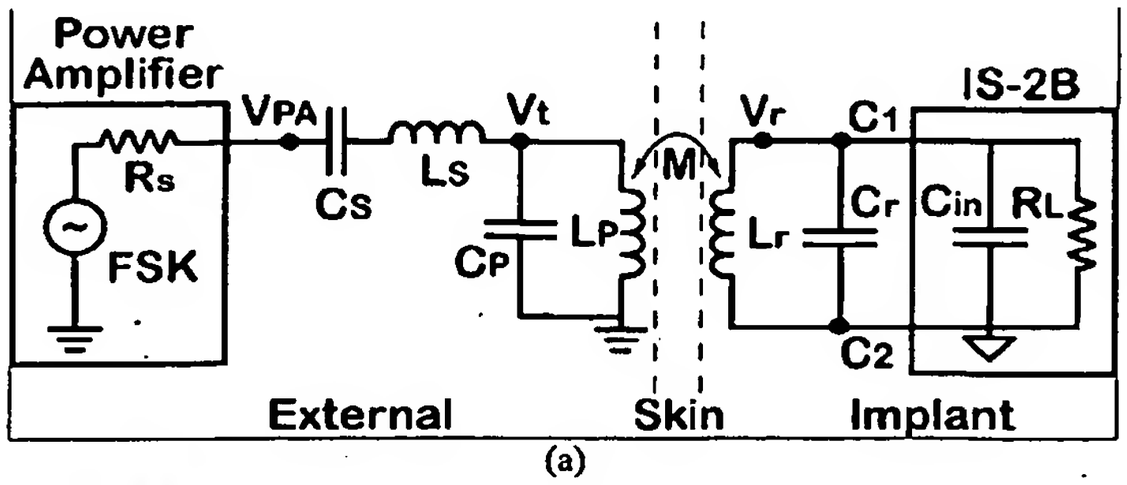
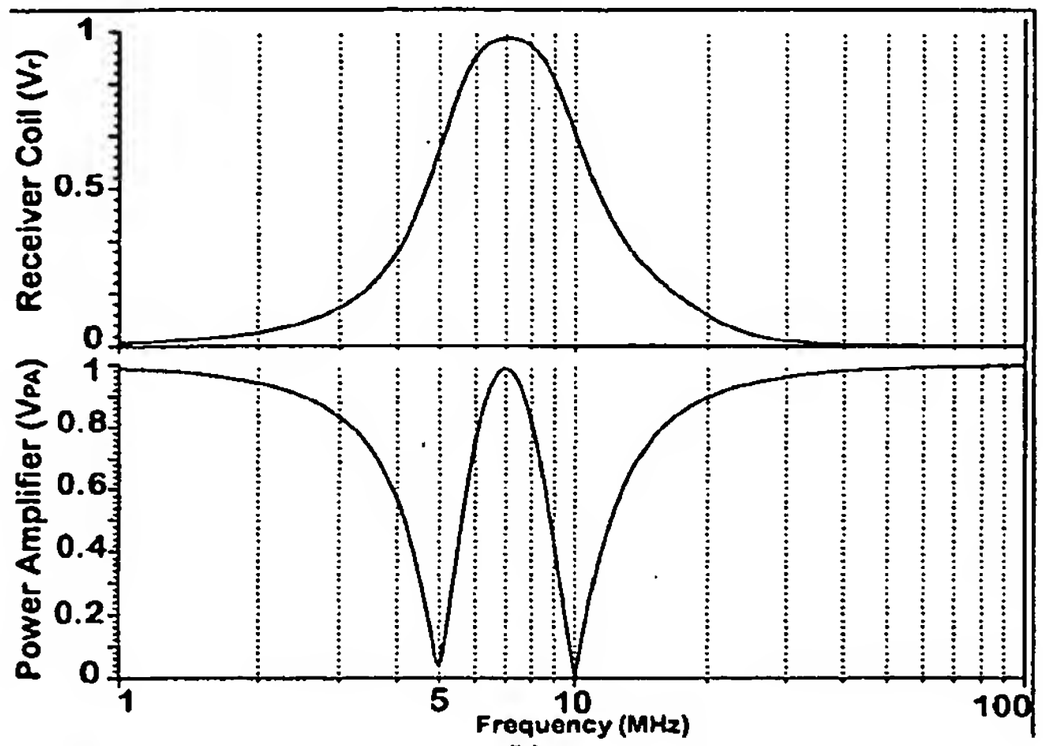


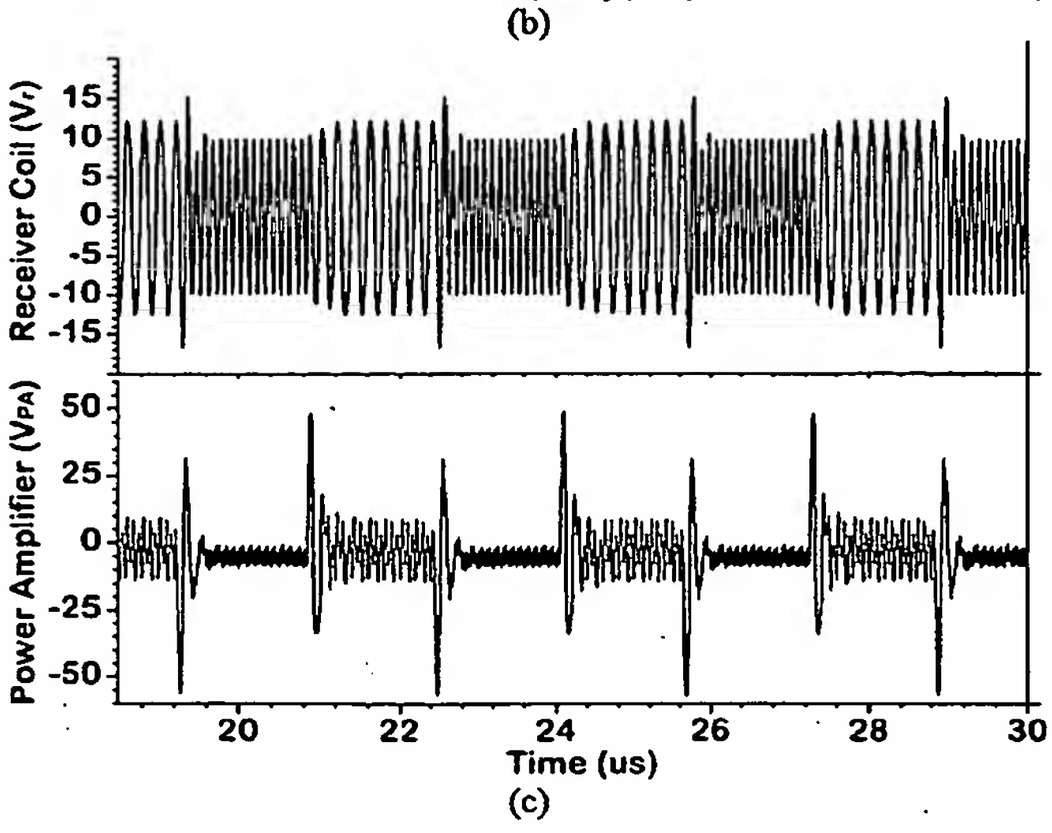
Fig. 8. The DFSK demodulator simulated waveforms.



(a)



(b)



(c)

Fig. 9. (a) Modeling of the combined series-parallel LC-tank with L_P used as the transmitter coil. (b) Simulated spectrum of the power amplifier output (V_{PA}) and the received signal (V_r) (c) V_{PA} and V_r simulated waveforms in time domain.

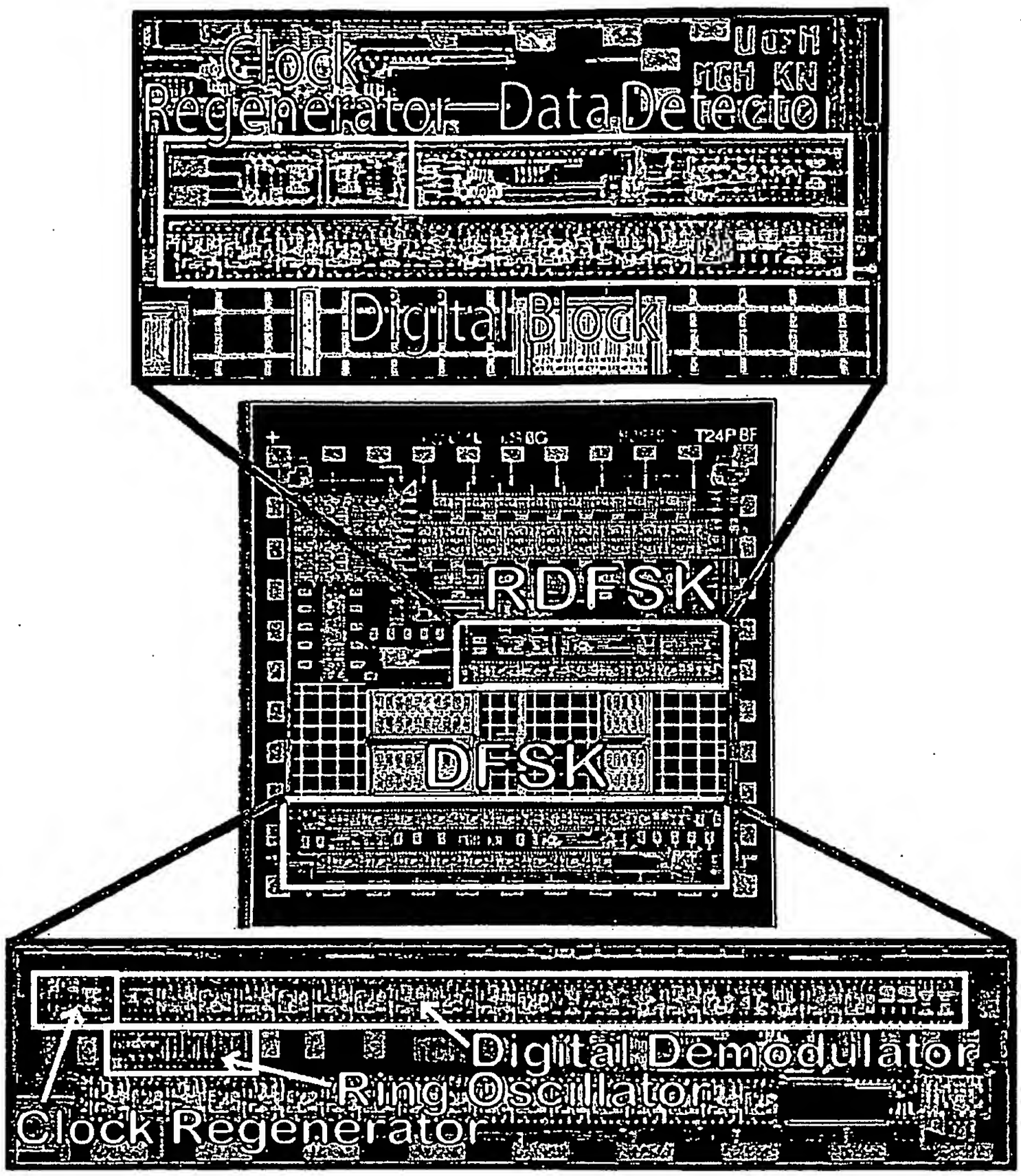


Fig. 10. The RDFSK and DFSK demodulators implemented in a prototype chip.

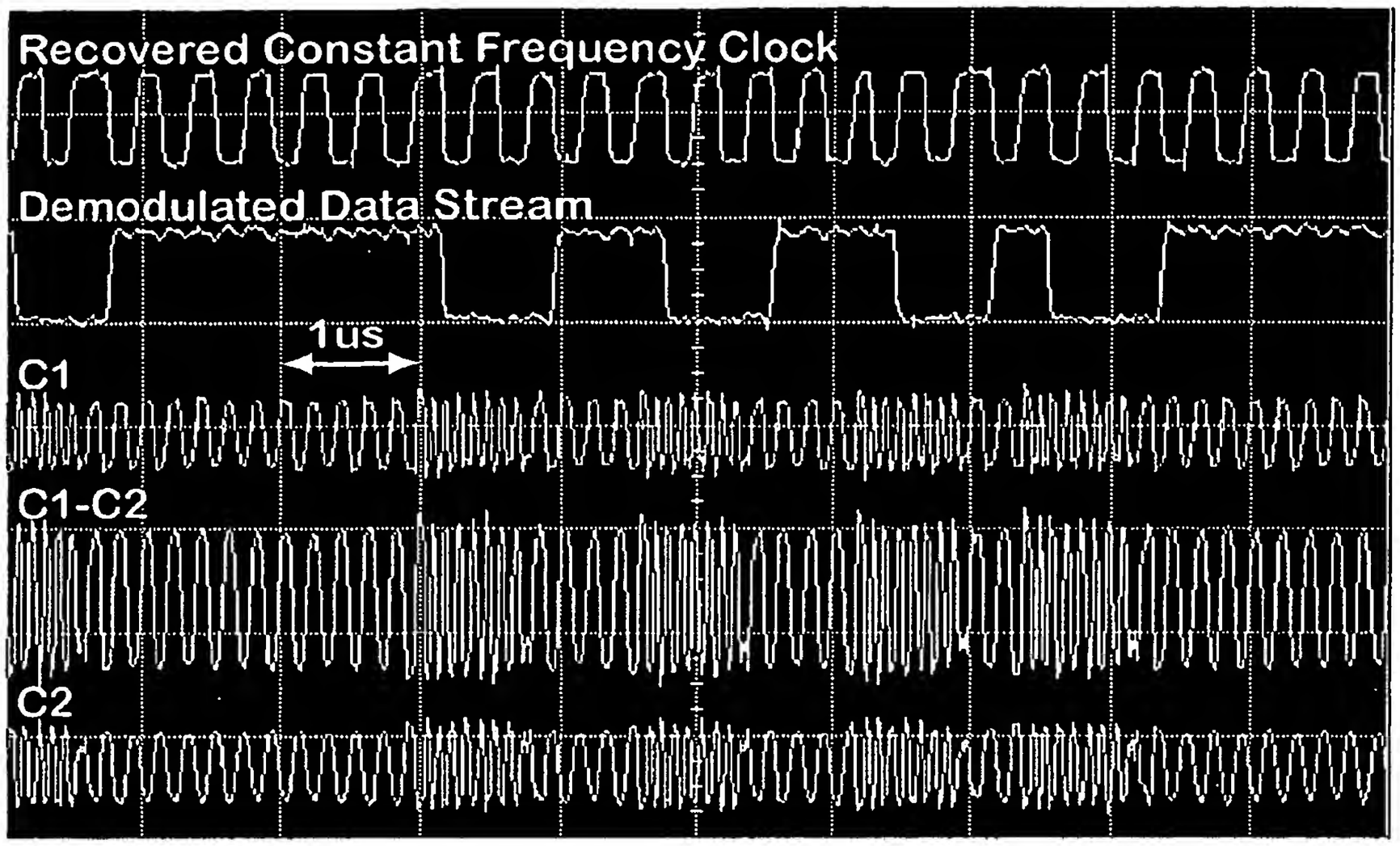


Fig. 11. The DFSK measured waveforms at 2.5Mbps with f_0 and f_1 equal to 10MHz and 5MHz, respectively. From top: Clock-Out, Data-Out, and single ended (C_1, C_2) and differential (C_1-C_2) carrier voltage at the receiver coil nodes [1μs/div].

TABLE 1
THE WIRELESS LINK CIRCUIT PARAMETERS

Parameter	Value	Comment
C_S	0.5nF	Series tank capacitor
L_S	1μH	Series tank inductor
C_P	1nF	Parallel tank capacitor
L_P	0.5μH	Parallel tank inductor
N_P	3	Parallel inductor turns
D_P	30mm	Parallel inductor diameter
C_r	10pF	Receiver tank capacitor
L_r*	9μH	Receiver tank inductor
N_r	15	Receiver inductor turns
D_r	12mm	Receiver inductor diameter
d_r	5mm	Distance between L_r and L_P planar coils
M	100nH	Mutual inductance between L_r and L_P
C_{in}	10pF	Wireless chip parasitic input capacitance
R_L	1kΩ	Wireless chip loading
R_S	50Ω	Transmitter output resistance

* The receiver coil has a ferrite core

TABLE 2
MEASURED RESULTS AND SPECIFICATIONS SUMMARY OF THE FSK DEMODULATOR CIRCUITS

Demodulation Technique	RDFSK	DFSK
Process technology	AMI 1.5-μm	AMI 1.5-μm
Die size (mm^2)	2.2 × 2.2	2.2 × 2.2
Circuit area (mm^2)	0.41	0.29
Carrier frequency range (MHz)	2 ~ 20	3.2 ~ 25
Max simulated data rate (Mbps)	4	4
Max measured data rate (Mbps)	1.5	2.5
C (pF)	1.2	-
I_C (μA)	40	-
V_{ref} (V)	1.26	-
Time-base clock (MHz)	-	50.5
Counter width (n)	-	3
Bit error rate at 2.5Mbps	-	10^{-5}
Supply voltage (V)	5	5
Power dissipation	0.45	0.38